Allen-Bradley

FLEX I/O Isolated Analog Modules

1794-IF4I, -OF4I, IF2XOF2I, -IF4IXT, -IF4ICFXT, -OF4IXT, IF2XOF2IXT

User Manual

Rockwell Automation

Important User Information

Solid state equipment has operational characteristics differing from those of electromechanical equipment. Safety Guidelines for the Application, Installation and Maintenance of Solid State Controls (publication SGI-1.1 available from your local Rockwell Automation sales office or online at http://literature.rockwellautomation.com) describes some important differences between solid state equipment and hard-wired electromechanical devices. Because of this difference, and also because of the wide variety of uses for solid state equipment, all persons responsible for applying this equipment must satisfy themselves that each intended application of this equipment is acceptable.

In no event will Rockwell Automation, Inc. be responsible or liable for indirect or consequential damages resulting from the use or application of this equipment.

The examples and diagrams in this manual are included solely for illustrative purposes. Because of the many variables and requirements associated with any particular installation, Rockwell Automation, Inc. cannot assume responsibility or liability for actual use based on the examples and diagrams.

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Throughout this manual, when necessary, we use notes to make you aware of safety considerations.S

WARNING	Identifies information about practices or circumstances that can cause an explosion in a hazardous environment, which may lead to personal injury or death, property damage, or economic loss.
IMPORTANT	Identifies information that is critical for successful application and understanding of the product.
ATTENTION	Identifies information about practices or circumstances that can lead to: personal injury or death, property damage, or economic loss. Attentions help you identify a hazard, avoid a hazard, and recognize the consequence.
SHOCK HAZARD	Labels may be on or inside the equipment, such as a drive or motor, to alert people that dangerous voltage may be present.
BURN HAZARD	Labels may be on or inside the equipment, such as a drive or motor, to alert people that surfaces may reach dangerous temperatures.

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Using this Manual

Purpose of this Manual

This manual shows you how to use your FLEX I/O Isolated Analog modules with Allen-Bradley programmable controllers. The manual helps you install, program and troubleshoot your modules.

Except where noted, information that applies to 1794-IF4I, 1794-OF4I, and IF2XOF2I also applies to 1794-IF4IXT, 1794-IF4ICFXT, 1794-OF4IXT, and IF2XOF2IXT.

Audience

You must be able to program and operate an Allen-Bradley programmable controller to make efficient use of your FLEX I/O modules. In particular, you must know how to program block transfers.

We assume that you know how to do this in this manual. If you do not, refer to the appropriate programming and operations manual before you attempt to program your modules.

Vocabulary

In this manual, we refer to:

- the isolated analog input or isolated analog output module as the “input module” or “output module”
- the Programmable Controller as the “controller”

Manual Organization

This manual is divided into five chapters. The following chart lists each chapter with its corresponding title and a brief overview of the topics covered in that chapter.

Section	Title	Contents
Chapter 1	Overview of FLEX I/O and your Analog Modules	Describes FLEX I/O Isolated Analog modules, features, and how they function
Chapter 2	How to Install Your Analog Module	How to install and wire the modules
Chapter 3	Module Programming	Explains block transfer programming, sample programs

Section	Title	Contents
Chapter 4	Writing Configuration to and Reading Status from Your Module with a Remote I/O Adapter	Explains how to configure your modules and read status information from your modules when using a remote I/O adapter
Chapter 5	Communication and I/O Image Table Mapping with the DeviceNet/ControlNet Adapter	Explains how you communicate with your modules, and how the I/O image is mapped when using a DeviceNet adapter
Chapter 6	Input, Output, Status and Configuration Files for Analog Modules when used with ControlNet	Explains how you communicate with your modules over ControlNet.
Chapter 7	Calibrating Your Module	Explains how to calibrate your module.
Appendix A	Specifications	Specifications for the isolated analog modules
Appendix B	Class I, Division 2, Group A, B, C, D Hazardous Locations Statement	Hazardous location approval

Common Techniques Used in this Manual

The following conventions are used throughout this manual:

- Bulleted lists such as this one provide information, not procedural steps.
- Numbered lists provide sequential steps or hierarchical information.

For Additional Information

For additional information on FLEX I/O systems and modules, refer to the following documents:

Catalog Numbers	Voltage	Description	Publications	
			Installation Instructions	User Manual
1794		1794 FLEX I/O Product Data	1794-2.1	
1794-ACN	24V dc	ControlNet Adapter	1794-5.8	
1794-ACNR	24V dc	Redundant Media ControlNet Adapter	1794-5.18	
1794-ADN	24V dc	DeviceNet Adapter	1794-5.14	1794-6.5.5
1794-ASB/C	24V dc	Remote I/O Adapter	1794-5.46	1794-6.5.9

Catalog Numbers	Voltage	Description	Publications	
			Installation Instructions	User Manual
1794-ASB2	24V dc	2-Slot Remote I/O Adapter	1794-5.44	1794-6.5.3
1794-TB2 1794-TB3		2-wire Terminal Base 3-wire Terminal Base	1794-5.2	
1794-TBN		Terminal Base Unit	1794-5.16	
1794-TBNF		Fused Terminal Base Unit	1794-5.17	
1794-TB3T		Temperature Terminal Base Unit	1794-5.41	
1794-TB3S		Spring Clamp Terminal Base Unit	1794-5.42	
1794-TB3TS		Spring Clamp Temperature Terminal Base Unit	1794-5.43	
1794-IB16	24V dc	16 Sink Input Module	1794-5.4	
1794-OB16	24V dc	16 Source Output Module	1794-5.3	
1794-IV16	24V dc	16 Source Input Module	1794-5.28	
1794-OV16	24V dc	16 Sink Output Module	1794-5.29	
1794-OB8EP	24V dc	8 Electronically Fused Output Module	1794-5.20	
1794-OW8	24V dc	8 Output Relay Module	1794-5.19	
1794-IB10XOB6	24V dc	10 Input/6 Output Module	1794-5.24	
1794-IE8	24V dc	Selectable Analog 8 Input Module	1794-5.6	
1794-OE4	24V dc	Selectable Analog 4 Output Module	1794-5.5	1794-6.5.2
1794-IE4XOE2	24V dc	4 Input/2 Output Analog Module	1794-5.15	
1794-IR8	24V dc	8 RTD Input Analog Module	1794-5.22	1794-6.5.4
1794-IT8	24V dc	8 Thermocouple Input Module	1794-5.21	1794-6.5.7
1794-IB8S	24V dc	Sensor Input Module	1794-5.7	
1794-IA8	120V ac	8 Input Module	1794-5.9	
1794-OA8	120V ac	Output Module	1794-5.10	
1794-CE1, -CE3		Extender Cables	1794-5.12	
1794-NM1		Mounting Kit	1794-5.13	
1794-PS1	24V dc	Power Supply	1794-5.35	
1794-PS13	24V dc	Power Supply	1794-5.69	

Summary

This preface gave you information on how to use this manual efficiently. The next chapter introduces you to the remote I/O adapter module.

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Overview of FLEX I/O and your Analog Modules

Chapter Objectives

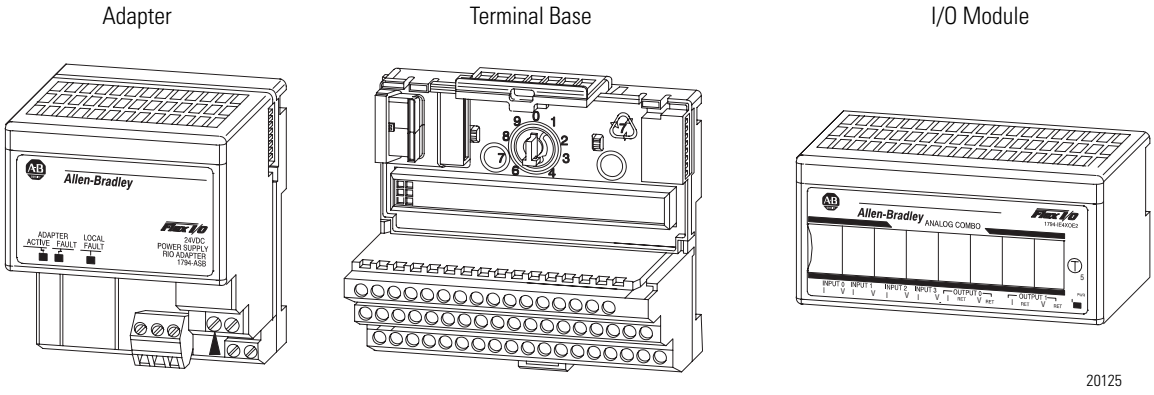
In this chapter, we tell you about:

- what the FLEX I/O system is and what it contains
- types of FLEX I/O analog modules
- how FLEX I/O analog modules communicate with programmable controllers
- the features of your analog modules

The FLEX I/O System

FLEX I/O is a small, modular I/O system for distributed applications that performs all of the functions of rack-based I/O. The FLEX I/O system contains the following components shown in Figure 1.1:

Figure 1.1



- adapter/power supply – powers the internal logic for as many as eight I/O modules
- terminal base – contains a terminal strip to terminate wiring for two- or three-wire devices
- I/O module – contains the bus interface and circuitry needed to perform specific functions related to your application

Types of FLEX I/O Modules

We describe the following FLEX I/O Analog modules in this user manual:

Catalog Number	Voltage	Inputs	Outputs	Description
1794-IF4I	24V dc	4	–	analog – 4 input, isolated
1794-OF4I	24V dc	–	4	analog – 4 output, isolated
1794-IF2XOF2I	24V dc	2	2	analog – 2 input, isolated and 2 output, isolated

FLEX I/O analog input, output and combination modules are block transfer modules that interface analog signals with any Allen-Bradley programmable controllers that have block transfer capability. Block transfer programming moves input from the module's memory to a designated area in the processor data table, and output data words from a designated area in the processor data table to the module's memory. Block transfer programming also moves configuration words from the processor data table to module memory.

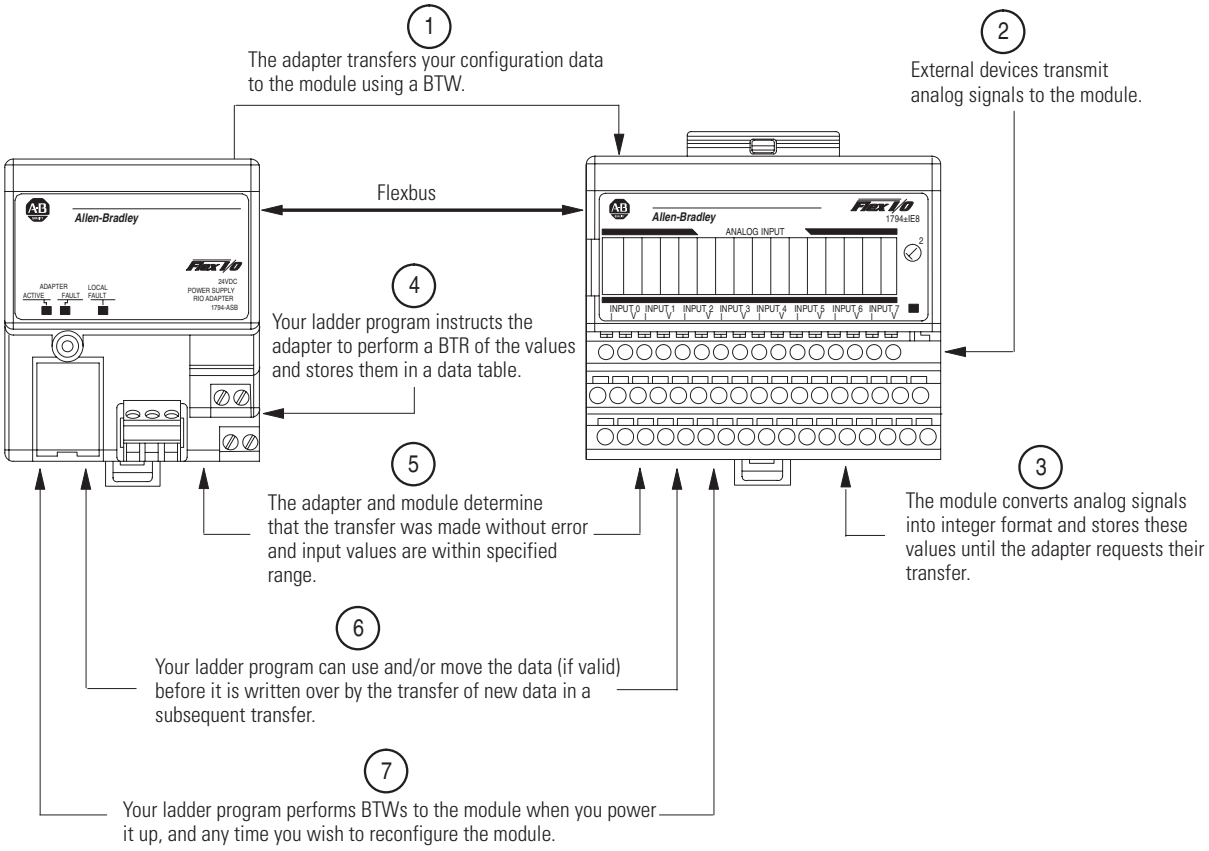
The analog modules have selectable ranges as shown in the table below:

Input Values	Data Format	Underrange/Overrange
4–20mA	signed 2's complement	4% Underrange, 4% Overrange
±10V	signed 2's complement	2% Underrange, 2% Overrange
±5V	signed 2's complement	4% Underrange, 4% Overrange
0–20mA	signed 2's complement %	0% Underrange, 4% Overrange
4-20mA	signed 2's complement %	4% Underrange, 4% Overrange
0–10V	signed 2's complement %	0% Underrange, 2% Overrange
±10V	signed 2's complement %	2% Underrange, 2% Overrange
0–20mA	binary	0% Underrange, 4% Overrange
4–20mA	binary	4% Underrange, 4% Overrange
0–10V	binary	0% Underrange, 2% Overrange
0–5V	binary	0% Underrange, 4% Overrange
±20mA	offset binary, 8000H = 0mA	4% Underrange, 4% Overrange
4–20mA	offset binary, 8000H = 4mA	4% Underrange, 4% Overrange
±10V	offset binary, 8000H = 0V	2% Underrange, 2% Overrange
±5V	offset binary, 8000H = 0V	4% Underrange, 4% Overrange

How FLEX I/O Analog Modules Communicate with Programmable Controllers

The adapter/power supply transfers data to the module (block transfer write) and from the module (block transfer read) using BTW and BTR instructions in your ladder diagram program. These instructions let the adapter obtain input values and status from the module, and let you send output values and establish the module's mode of operation. Figure 1.2 describes the communication process.

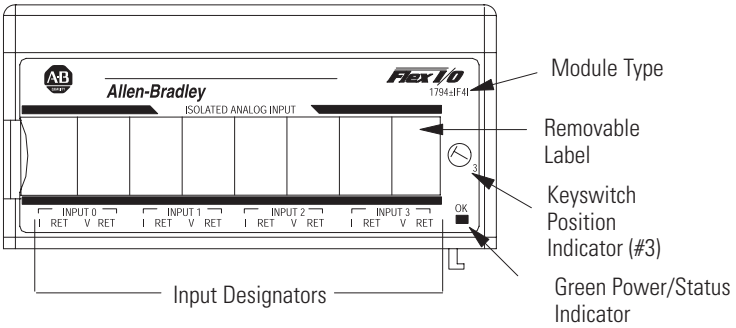
Figure 1.2
An Example of Communication Between an Adapter and an Analog Input Module



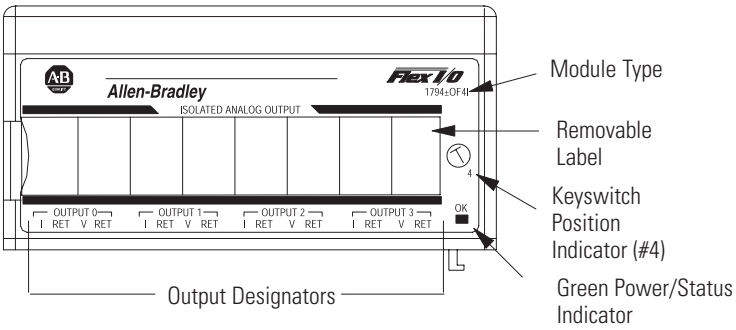
Features of Your Analog Modules

Each module has a unique label identifying its keyswitch position, wiring and module type. A removable label provides space for writing individual designations per your application.

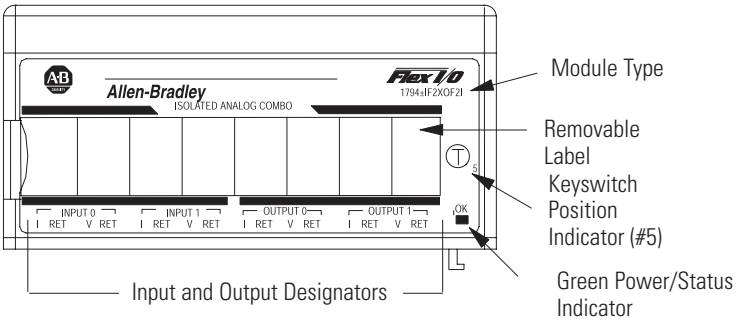
1794-IF4I



1794-OF4I



1794-IF2XOF2I



Summary

In this chapter you learned about the FLEX I/O system and the types of analog modules and how they communicate with programmable controllers.

How to Install Your Analog Module

Chapter Objectives

In this chapter, we tell you about:

- how to install your module
- how to set the module keyswitch
- how to wire the terminal base
- the indicators

Before You Install Your Analog Module

Before installing your analog module in the I/O chassis:

You need to:	As described under:
Calculate the power requirements of all modules in each chassis.	Power Requirements, page 2-16
Position the keyswitch on the terminal base	Mounting the Analog Module on the Terminal Base Unit, page 2-22

Compliance to European Union Directives

If this product has the CE mark it is approved for installation within the European Union and EEA regions. It has been designed and tested to meet the following directives.

EMC Directive

This product is tested to meet Council Directive 2004/10/EC Electromagnetic Compatibility (EMC) and the following standards, in whole or in part, documented in a technical construction file:

- European Union 2004/108/EC EMC Directive, compliant with:
  EN 61326-1; Meas./Control/Lab., Industrial Requirements
  EN 61000-6-2; Industrial Immunity
  EN 61000-6-4; Industrial Emissions
  EN 61131-2; Programmable Controllers (Clause 8, Zone A & B)
- European Union 2006/95/EC LVD, compliant with:
  EN 61131-2; Programmable Controllers (Clause 11)

This product is intended for use in an industrial environment.

Low Voltage Directive

This product is tested to meet Council Directive 2006/95/EC Low Voltage, by applying the safety requirements of EN 61131–2 Programmable Controllers, Part 2 – Equipment Requirements and Tests.

For specific information required by EN 61131-2, see the appropriate sections in this publication, as well as the following Allen-Bradley publications:

- Industrial Automation Wiring and Grounding Guidelines For Noise Immunity, publication 1770-4.1
- Guidelines for Handling Lithium Batteries, publication AG-5.4
- Automation Systems Catalog, publication B111

Open style devices must be provided with environmental and safety protection by proper mounting in enclosures designed for specific application conditions. See NEMA Standards publication 250 and IEC publication 529, as applicable, for explanations of the degrees of protection provided by different types of enclosure.

Power Requirements

The wiring of the terminal base unit is determined by the current draw through the terminal base. Make certain that the current draw does not exceed 10A.

ATTENTION

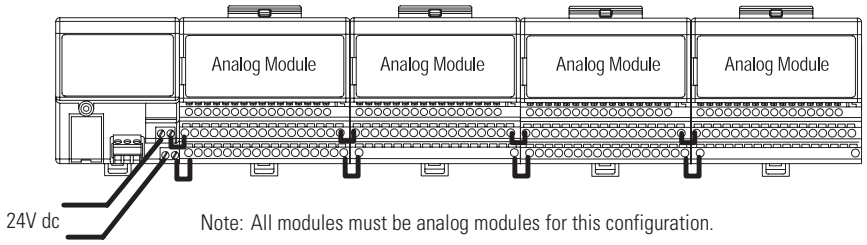
Total current draw through the terminal base unit is limited to 10A. Separate power connections may be necessary.

Methods of wiring the terminal base units are shown in the illustration below.

ATTENTION

Do not daisy chain power or ground from an analog terminal base unit to any ac or dc discrete module terminal base unit.

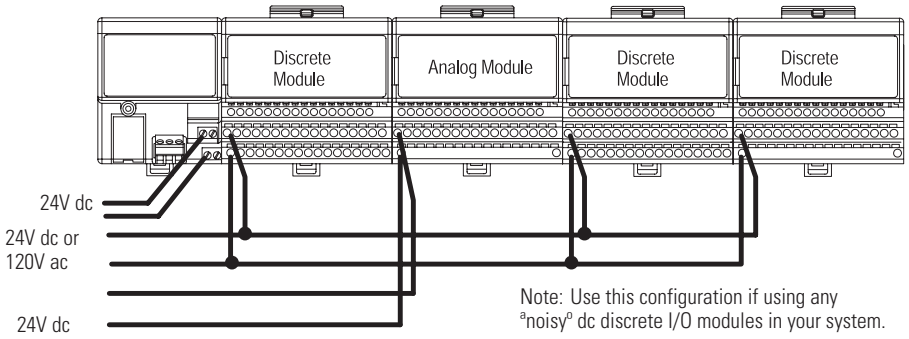
Daisy-chaining



Note: All modules must be analog modules for this configuration.

Wiring when total current draw is less than 10A

Individual

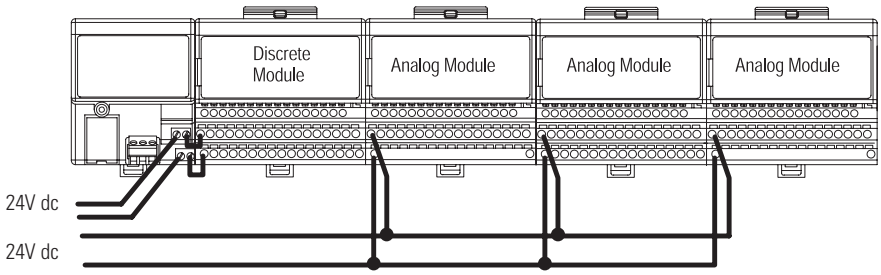


Note: Use this configuration if using any [a]noisy[a] dc discrete I/O modules in your system.

Analog module wiring separate from discrete wiring.

Wiring when total current draw is greater than 10A

Combination



Note: All modules powered by the same power supply must be analog modules for this configuration.

Total current draw through any base unit must not be greater than 10A

Installing the Module

Installation of the analog module consists of:

- mounting the terminal base unit
- installing the analog module into the terminal base unit
- installing the connecting wiring to the terminal base unit

If you are installing your module into a terminal base unit that is already installed, proceed to Mounting the Analog Module on the Terminal Base Unit on page 2-22.

Mounting the Terminal Base Unit on a DIN Rail

ATTENTION

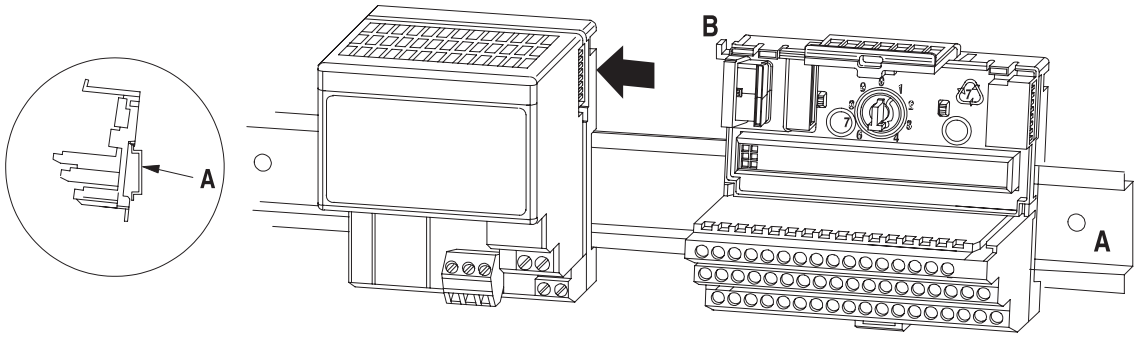
Do not remove or replace a terminal base unit when power is applied. Interruption of the flexbus can result in unintended operation or machine motion.

1. Remove the cover plug (if used) in the male connector of the unit to which you are connecting this terminal base unit.

2. Check to make sure that the 16 pins in the male connector on the adjacent device are straight and in line so that the mating female connector on this terminal base unit will mate correctly.

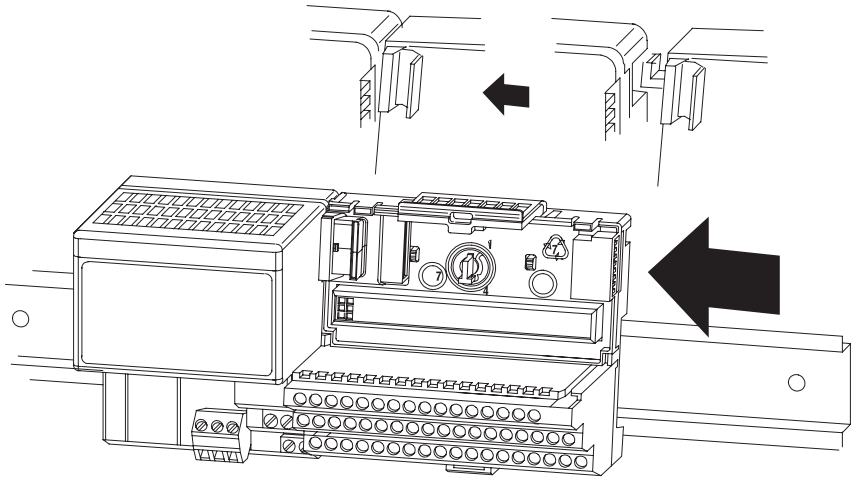
3. Position the terminal base on the 35 x 7.5mm DIN rail **A** (A-B pt. no. 199-DR1; 46277-3; EN 50022) at a slight angle with hook **B** on the left side of the terminal base hooked into the right side of the unit on the left. Proceed as follows:

Figure 2.1

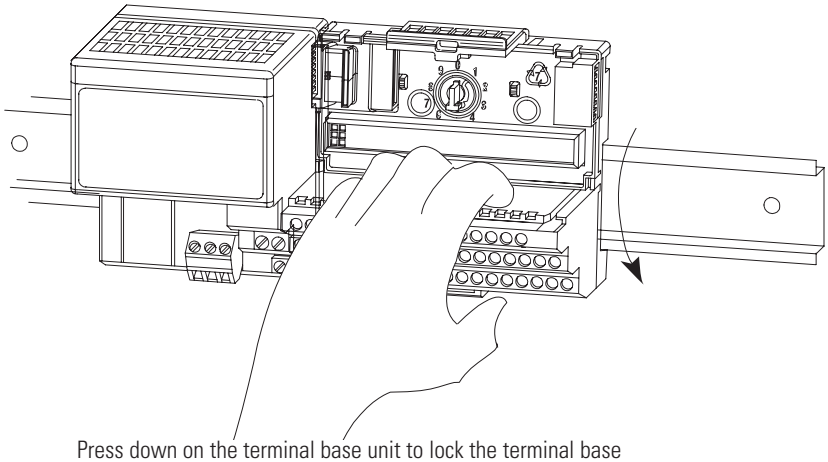


Position terminal base at a slight angle and hooked over the top of the DIN rail.

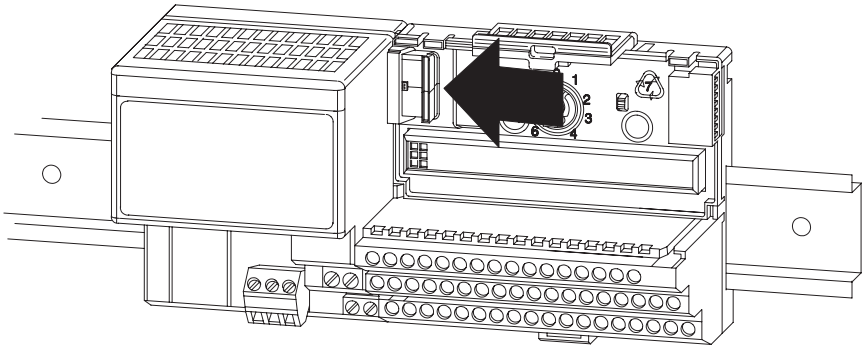
Figure 2.2



Slide the terminal base unit over tight against the adapter. Make sure the hook on the terminal base slides under the edge of the adapter and the flexbus connector is fully retracted.



Press down on the terminal base unit to lock the terminal base on the DIN rail. If the terminal base does not lock into place, use a screwdriver or similar device to open the locking tab, press down on the terminal base until flush with the DIN rail and release the locking tab to lock the base in place.



Gently push the flexbus connector into the side of the adapter to complete the backplane connection.

30077-M

4. Repeat steps 1 - 3 to install the next terminal base.

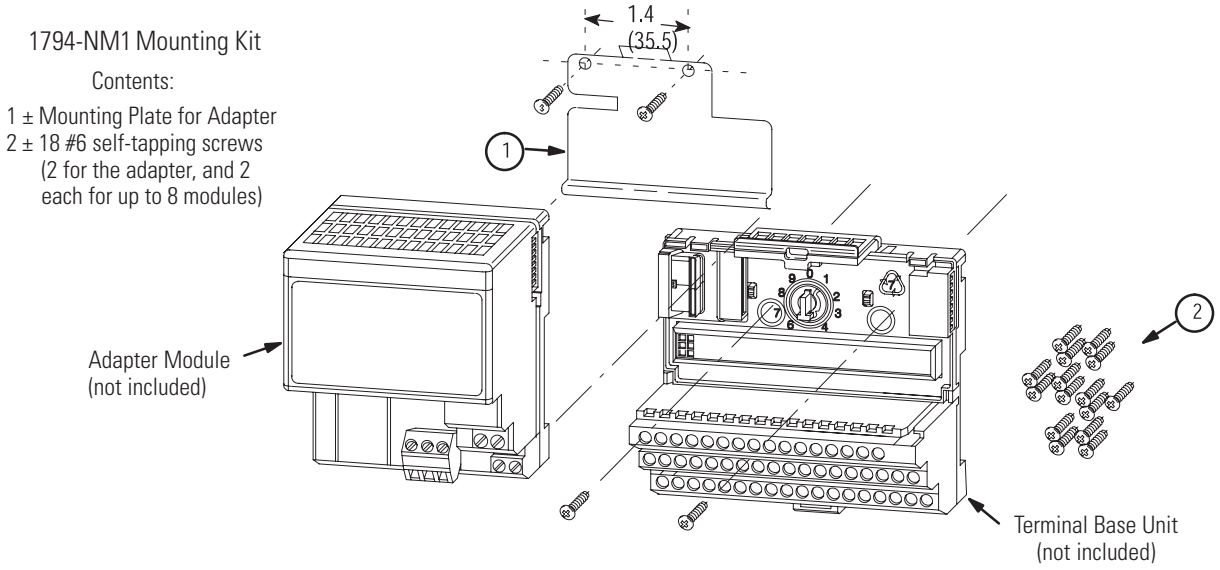
Panel/Wall Mounting

Installation on a wall or panel consists of:

- laying out the drilling points on the wall or panel
- drilling the pilot holes for the mounting screws
- mounting the adapter mounting plate
- installing the terminal base units and securing them to the wall or panel

If you are installing your module into a terminal base unit that is already installed, proceed to “Mounting the Analog Module on the Terminal Base” on .

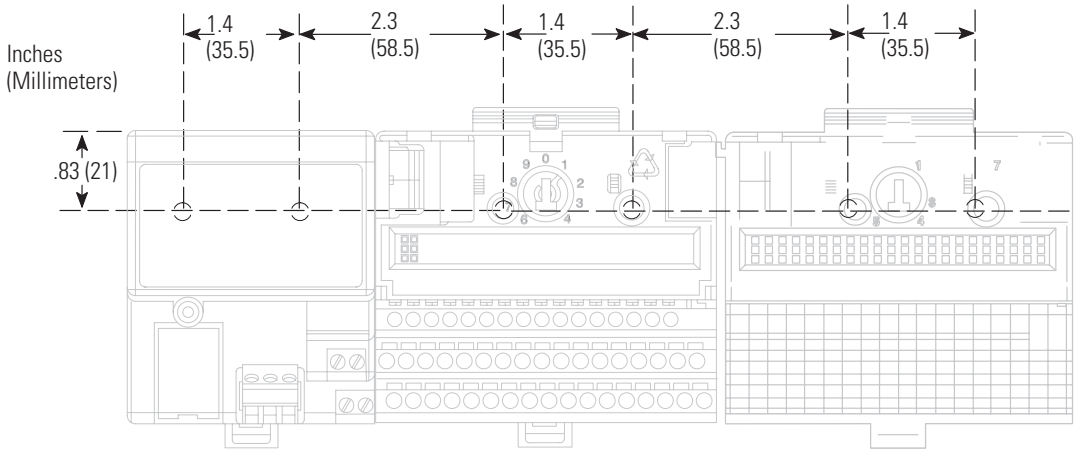
Use the mounting kit Cat. No. 1794-NM1 for panel/wall mounting.



To install the mounting plate on a wall or panel:

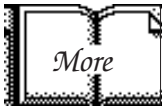
1. Lay out the required points on the wall/panel as shown in the drilling dimension drawing.

Figure 2.3 Drilling Dimensions for Panel/Wall Mounting of FLEX I/O



2. Drill the necessary holes for the #6 self-tapping mounting screws.

3. Mount the mounting plate (1) for the adapter module using two #6 self-tapping screws (18 included for mounting up to 8 modules and the adapter).



IMPORTANT Make certain that the mounting plate is properly grounded to the panel. Refer to "Industrial Automation Wiring and Grounding Guidelines," publication 1770-4.1.

4. Hold the adapter (2) at a slight angle and engage the top of the mounting plate in the indention on the rear of the adapter module.

5. Press the adapter down flush with the panel until the locking lever locks.

6. Position the terminal base unit up against the adapter and push the female bus connector into the adapter.

7. Secure to the wall with two #6 self-tapping screws.

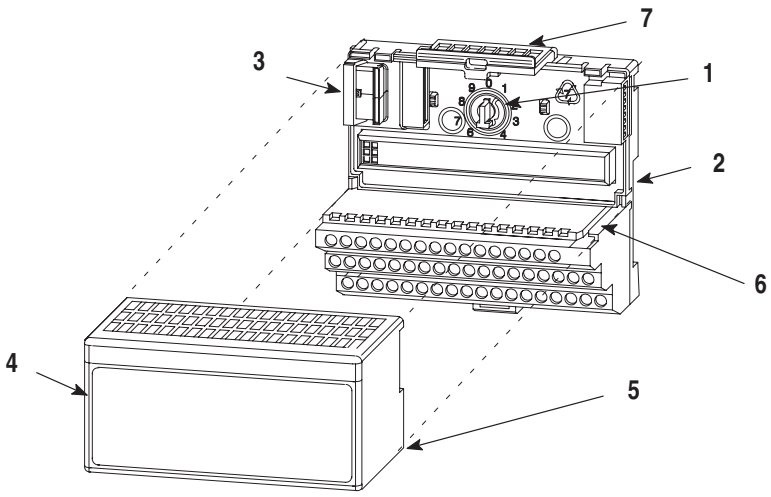
8. Repeat for each remaining terminal base unit.

   The adapter is capable of addressing eight modules. Do not exceed a maximum of eight terminal base units in your system.

Mounting the Analog Module on the Terminal Base Unit

1. Rotate the keyswitch (1) on the terminal base unit (2) clockwise to the position required for the specific type of analog module.

Figure 2.4



Analog Module Catalog Number	Keyswitch Position
1794-IF4I, 1794-IF4IXT, 1794-IF4ICFXT	3
1794-OF4I, 1794-OF4IXT	4
1794-IF2XOF2I, 1794-IF2XOF2IXT	5

2. Make certain the flexbus connector (3) is pushed all the way to the left to connect with the neighboring terminal base/adapter. **You cannot install the module unless the connector is fully extended.**

3. Make sure that the pins on the bottom of the module are straight so they will align properly with the connector in the terminal base unit.

4. Position the module (4) with its alignment bar (5) aligned with the groove (6) on the terminal base.

5. Press firmly and evenly to seat the module in the terminal base unit. The module is seated when the latching mechanism (7) is locked into the module.

6. Repeat the above steps to install the next module in its terminal base unit.

ATTENTION

Remove field-side power before removing or inserting the module. This module is designed so you can remove and insert it under backplane power. When you remove or insert a module with field-side power applied, an electrical arc may occur. An electrical arc can cause personal injury or property damage by:

- sending an erroneous signal to your system's field devices causing unintended machine motion
- causing an explosion in a hazardous environment

Repeated electrical arcing causes excessive wear to contacts on both the module and its mating connector. Worn contacts may create electrical resistance.

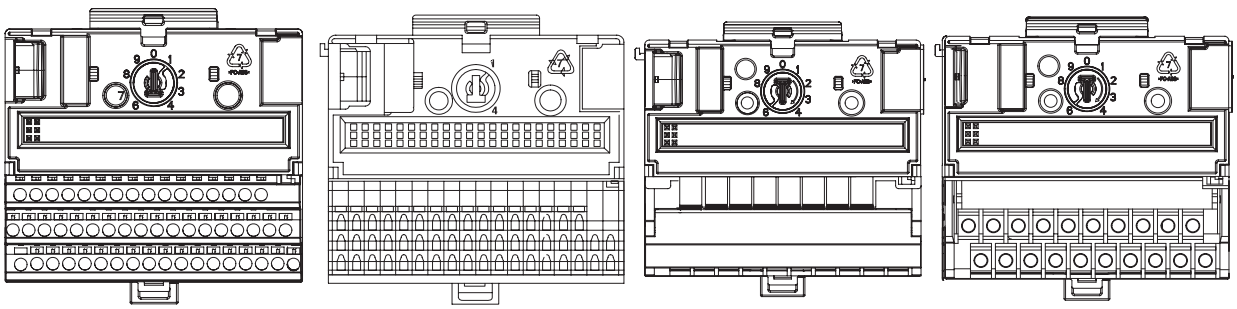
Connecting Wiring for the Analog Modules

Wiring to the analog modules is made through the terminal base unit on which the module mounts.

Refer to the following table for recommended terminal base units that you can use for each module.

Module	1794-TB3	1794-TBT	1794-TB3S	1794-TB3TS	1794-TB3S	1794-TBN, -TBNF
1794-IF4I, 1794-IF4IXT, 1794-IF4ICFXT	Yes	Yes	Yes	Yes	Yes	Yes
1794-OF4I, 1794-OF4IXT	Yes	Yes	Yes	Yes	Yes	Yes
1794-IF2XOF2I, 1794-IF2XOF2IXT	Yes	Yes	Yes	Yes	Yes	Yes

Figure 2.5



1794-TB3, -TB3T 1794-TB3S, -TB3TS 1794-TBNF 1794-TBN

Connecting wiring for the individual analog modules is shown on:

Module	Connecting Wiring
1794-IF4I, 1794-IF4IXT, 1794-IF4ICFXT	page 2-26
1794-OF4I, 1794-OF4IXT	
1794-IF2XOF2I, 1794-IF2XOF2IXT	page 2-27

Connecting Wiring using a 1794-TB3, -TB3T, -TB3S or -TB3TS Terminal Base Unit

1. Connect the individual signal wiring to numbered terminals on the **0–15** row **(A**) on the terminal base unit. (Use Belden 8761 cable for signal wiring.)

ATTENTION

Connect only one current or one voltage signal per channel. Do not connect both current and voltage on one channel.

2. Connect each channel signal return to:

   1794-IF4I – the associated terminal on row **A**.

   1794-OF4I – the corresponding terminal on the same row **(A)**

   1794-IF4XOF2I – inputs – the associated terminal on row **A;** outputs – the corresponding terminal on the same row **(A).**

3. Refer to Table 2.1 or Table 2.2. Connect +24V dc to designated terminals on the **34-51** row **(C)**, and 24V common todesignated terminals on the **16–33** row **(B)**.

ATTENTION

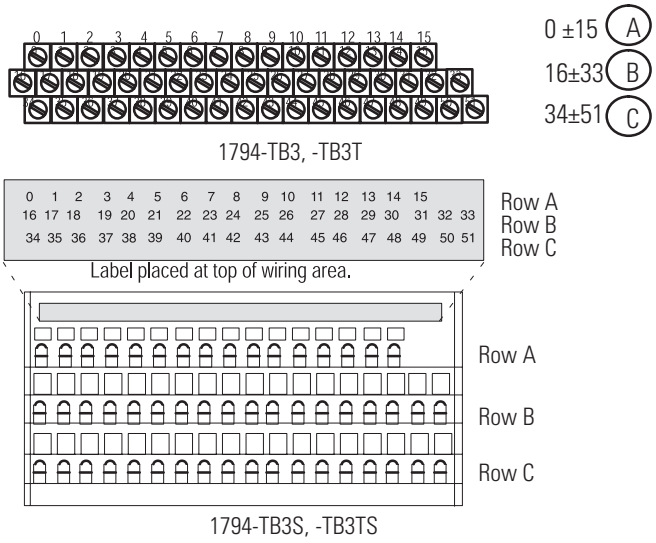
To reduce susceptibility to noise, power analog modules and discrete modules from separate power supplies. Do not exceed a length of 33 ft (10m) for dc power cabling.

ATTENTION

Remove field-side power before removing or inserting the module. This module is designed so you can remove and insert it under backplane power. When you remove or insert a module with field-side power applied, an electrical arc may occur. An electrical arc can cause personal injury or property damage by:

- sending an erroneous signal to your system's field devices causing unintended machine motion
- causing an explosion in a hazardous environment

Repeated electrical arcing causes excessive wear to contacts on both the module and its mating connector. Worn contacts may create electrical resistance.



4. If daisy chaining the +24V dc power to the next base unit, connect a jumper from terminal 51 on this base unit to terminal 34 on the next base unit. Connect the 24V dc common/return from terminal 33 on this base unit to terminal 16 on the next base unit.

Wiring to a 1794-TBN or 1794-TBNF Terminal Base Unit

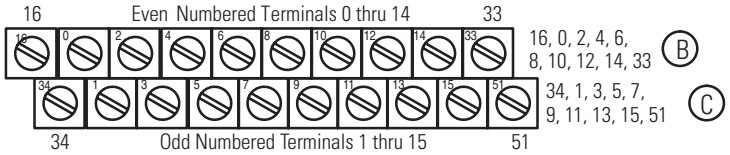
1. Connect individual input or output wiring to the even numbered terminals on row **(**B**)** as indicated in the table below.

2. Connect the associated return wiring to the corresponding odd numbered terminal on row (C) for each input or output as indicated in the table below.

3. Connect 24V dc to terminal 34 on row **(C)**.

4. Connect 24V dc common to terminal 16 on row **(B)**.

5. If continuing power to the next terminal base unit, connect a jumper from terminal 51 (24V dc) on this base unit to terminal 34 on the next base unit.



1794-TBN, 1794-TBNF

If continuing common to the next terminal base unit, connect a jumper from terminal 33 (24V dc common) on this base unit to terminal 16 on the next base unit.

Table 2.1
Wiring connections for 1794-TB3, -TB3T, -TB3S, -TB3TS, -TBN and -TBNF Terminal Base Units when using the 1794-IF4I or 1794-OF4I Isolated Analog Module

Channel	Signal Type	Label Markings	1794-TB3, -TB3T1, -TB3S, -TB3TS(2) 1794-TBN, 1794-TBNF	
			Signal Terminal	Signal Return
0	Current	I0	0	
	Current	I0 Ret		1
	Voltage	V0	2	
	Voltage	V0 Ret		3
1	Current	I1	4	
	Current	I1 Ret		5
	Voltage	V1	6	
	Voltage	V1 Ret		7

Table 2.1
Wiring connections for 1794-TB3, -TB3T, -TB3S, -TB3TS, -TBN and -TBNF Terminal Base Units when using the 1794-IF4I or 1794-OF4I Isolated Analog Module

Channel	Signal Type	Label Markings	1794-TB3, -TB3T1, -TB3S, -TB3TS(2) 1794-TBN, 1794-TBNF	
			Signal Terminal	Signal Return
2	Current	I2	8	
	Current	I2 Ret		9
	Voltage	V2	10	
	Voltage	V2 Ret		11
3	Current	I3	12	
	Current	I3 Ret		13
	Voltage	V3	14	
	Voltage	V3 Ret		15
	24V dc Common	1794-TB3 – 16 through 33(1) 1794-TB3T, -TB3TS – 17, 18, 33 1794-TBN, -TBNF – 16 and 33		
	+24V dc power	1794-TB3 – 34 thru 51 1794-TB3T, -TB3TS – 34, 35, 50, 51 1794-TBN, -TBNF – 34 and 51		

(1) Terminals 16 thru 33 are internally connected in the terminal base unit.

(2) Terminal 39 through 46 are chassis ground. Terminals 36, 37, 38 and 47, 48, 49 are used or cold junction compensation.

Table 2.2
Wiring connections for the 1794-IF2XOF2I Isolated Analog Module when using 1794-TB3, -TB3T, -TB3S, -TB3TS, -TBN and -TBNF Terminal Base Units

Channel	Signal Type	Label Markings	1794-TB3, -TB3T(2), -TB3S, -TB3TS(2) -TBN, -TBNF	
			Signal Terminal	Signal Return
Input 0	Current	I0	0	
	Current	I0 Ret		1
	Voltage	V0	2	
	Voltage	V0 Ret		3
Input 1	Current	I1	4	
	Current	I1 Ret		5
	Voltage	V1	6	
	Voltage	V1 Ret		7

Table 2.2
Wiring connections for the 1794-IF2XOF2I Isolated Analog Module when using 1794-TB3, -TB3T, -TB3S, -TB3TS, -TBN and -TBNF Terminal Base Units

Channel	Signal Type	Label Markings	1794-TB3, -TB3T[2], -TB3S, -TB3TS[2] -TBN, -TBNF	
			Signal Terminal	Signal Return
Output 0	Current	I2	8	
	Current	I2 Ret		9
	Voltage	V2	10	
	Voltage	V2 Ret		11
Output 1	Current	I3	12	
	Current	I3 Ret		13
	Voltage	V3	14	
	Voltage	V3 Ret		15
	24V dc Common	1794-TB3 – 16 thru 33[1] 1794-TB3T, -TB3TS – 17, 18, 33 1794-TBN, -TBNF – 16 and 33		
	+24V dc power	1794-TB3 – 34 thru 51 1794-TB3T, -TB3TS – 34, 35, 50, 51 1794-TBN, -TBNF – 34 and 51		

(1) Terminals 16 thru 33 are internally connected in the terminal base unit.

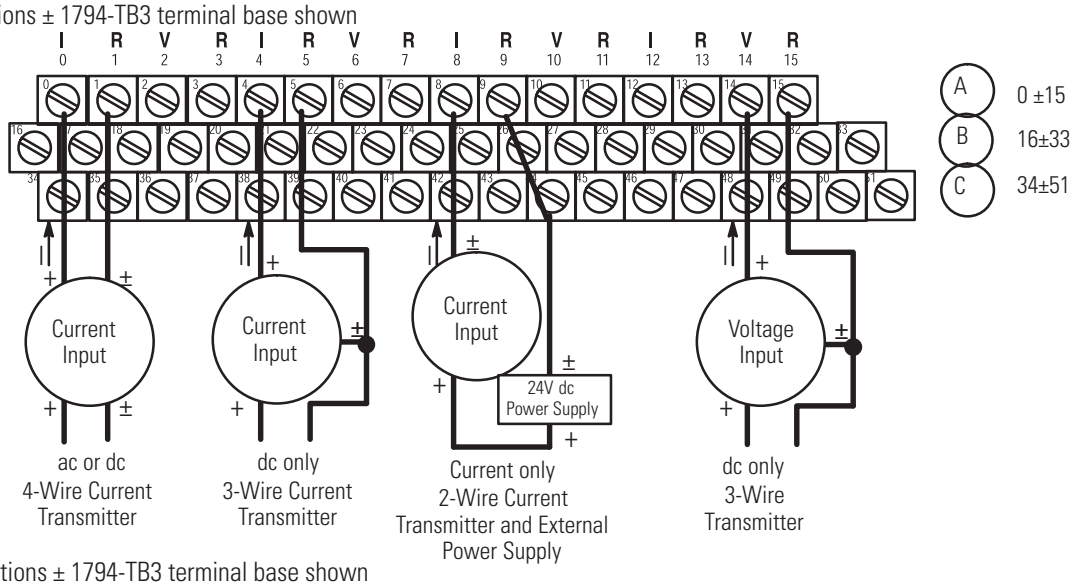
(2) Terminal 39 through 46 are chassis ground. Terminals 36, 37, 38 and 47, 48, 49 are used or cold junction compensation.

ATTENTION

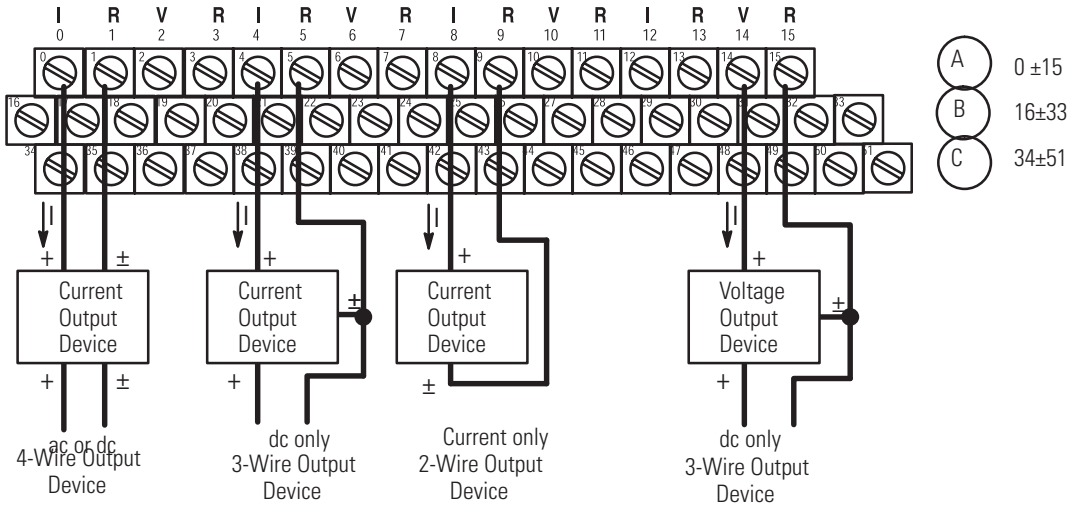
Total current draw through the terminal base unit is limited to 10A. Separate power connections to the terminal base unit may be necessary.

Figure 2.6

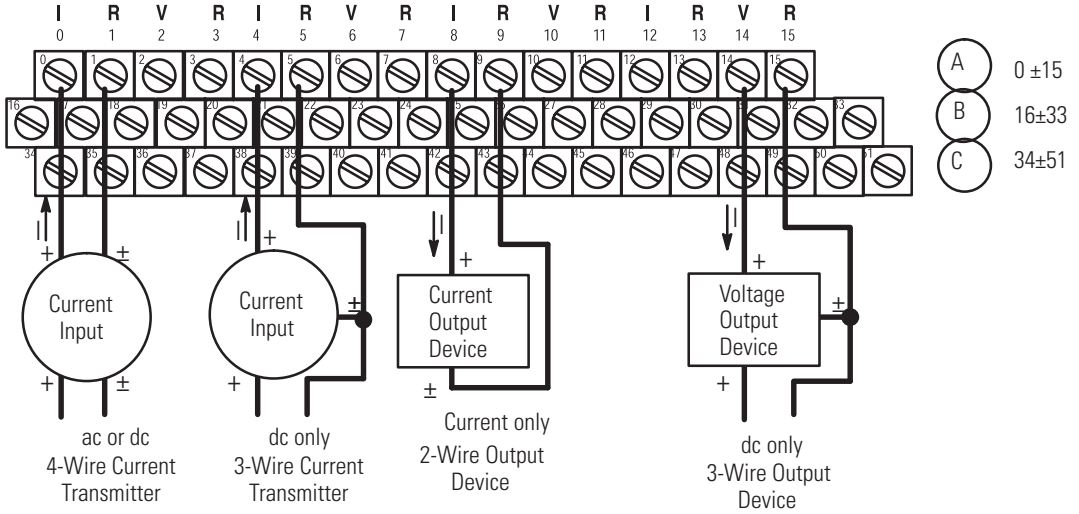
1794-IF4I Connections ± 1794-TB3 terminal base shown



1794-OF4I Connections ± 1794-TB3 terminal base shown

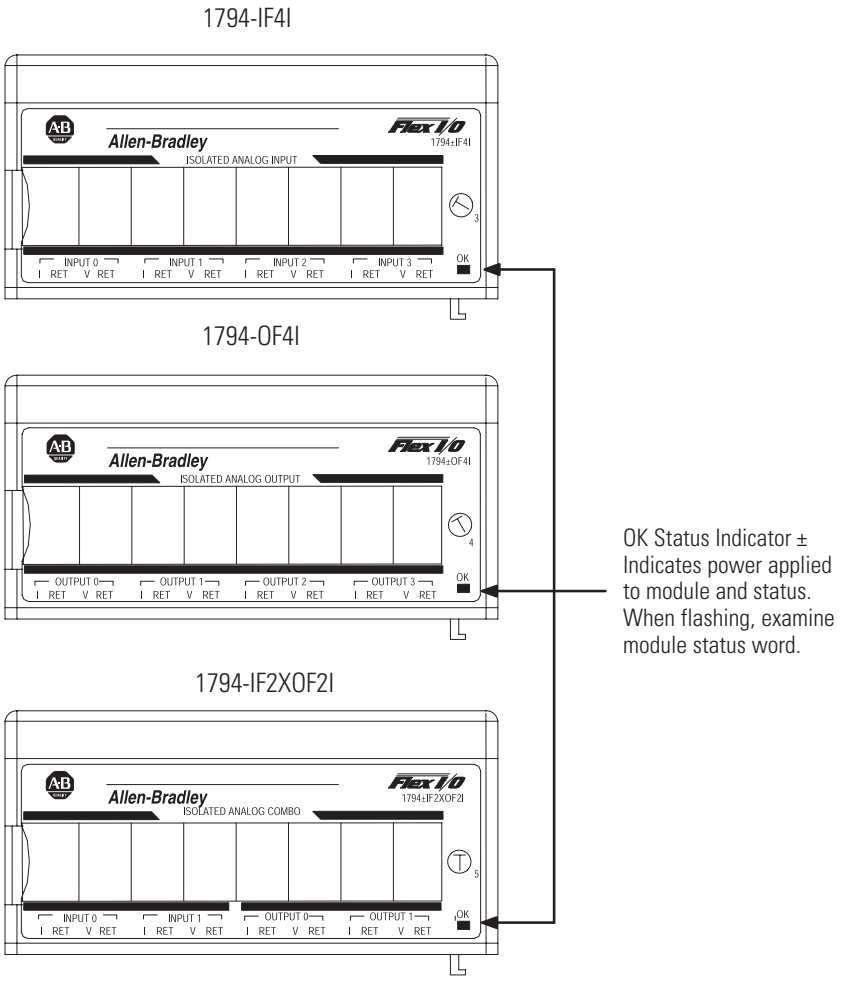


1794-IF2XOF2I Connections ± 1794-TB3 terminal base shown



Module Indicators

The analog modules have one status indicator that is on when power is applied to the module.



Chapter Summary

In this chapter you learned how to install your input module in an existing programmable controller system and how to wire to the terminal base units.

Module Programming

Chapter Objectives

In this chapter, we tell you about:

- analog data format
- block transfer programming
- configuration rungs
- sample programs for the PLC-3 and PLC-5 processors

Block Transfer Programming

Your module communicates with the processor through bidirectional block transfers. This is the sequential operation of both read and write block transfer instructions.

A configuration block transfer write (BTW) is initiated when the analog module is first powered up, and subsequently only when the programmer wants to enable or disable features of the module. The configuration BTW sets the bits which enable the programmable features of the module, such as filters and signal ranges, etc. Block transfer reads are performed to retrieve information from the module.

Block transfer read (BTR) programming moves status and data from the module to the processor's data table. The processor user program initiates the request to transfer data from the module to the processor. The transferred words contain module status, channel status and input data from the module.

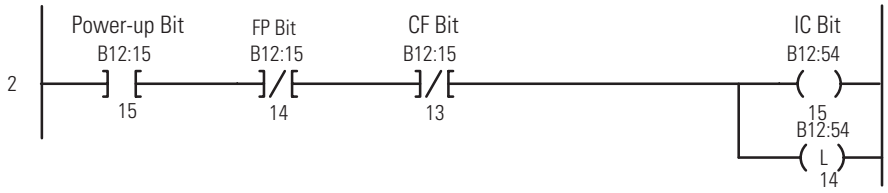
The following sample programs are minimum programs; all rungs and conditioning must be included in your application program. You can disable BTRs, or add interlocks to prevent writes if desired. Do not eliminate any storage bits or interlocks included in the sample programs. If interlocks are removed, the program may not work properly.

Your program should monitor status bits, block transfer read and block transfer write activity.

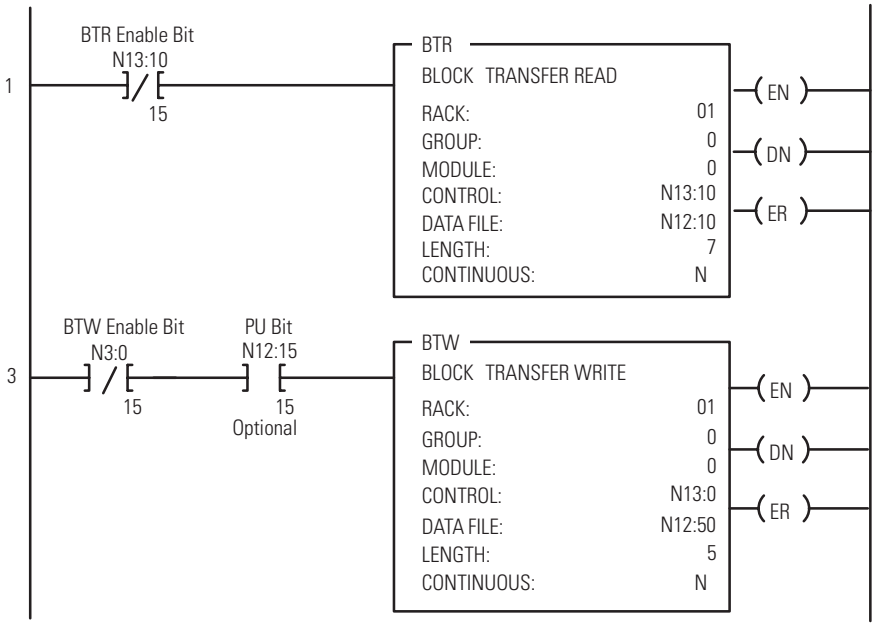
Configuration Rungs

Example Configuration Rungs

It is necessary to toggle the IC bit[1] (initiate configuration) for the isolated analog modules to accept configuration data. Once the configuration data has been properly set up, the following rung will reconfigure the module (this example represents sizes for the 1794-IF4I module).



If there are rungs which already perform reads and writes to the module, no additional rungs are necessary. A simplified example of a BTR and BTW rung for an 1794-IF4I follow (the 1794-OF4I is read length 6, write length 7; the 1794-IF2XOF2I is read length 7, write length 7):



An XIC (—] [—) instruction of the Power Up bit (PU) can be inserted to allow BTWs only when the module requires configuration (PU = 1).

(1) For systems that do not require ladder program control of configuration, set the TR bit (bit 13) to 1. Refer to Chapter 1.

Sample Programs for FLEX I/O Analog Modules

The following sample programs show you how to use your analog module efficiently when operating with a programmable controller. These programs show you how to:

- configure the module
- read data from the module
- update the module's output channels (if used)

With RSLogix5000, just read or write the tags provided. RSLogix will perform the transfer so an explicit block transfer is not required.

These programs illustrate the minimum programming required for communication to take place.

PLC-3 Programming

Block transfer instructions with the PLC-3 processor use one binary file in a data table section for module location and other related data. This is the block transfer control file. The block transfer data file stores data that you want transferred to your module (when programming a block transfer write) or from your module (when programming a block transfer read). The address of the block transfer data files are stored in the block transfer control file.

The same block transfer control file is used for both the read and write instructions for your module. A different block transfer control file is required for every module.

A sample program segment with block transfer instructions is shown in Figure 1.1, and described below.

Figure 1.1
PLC-3 Family Sample Program Structure for a 1794-IF4I Module

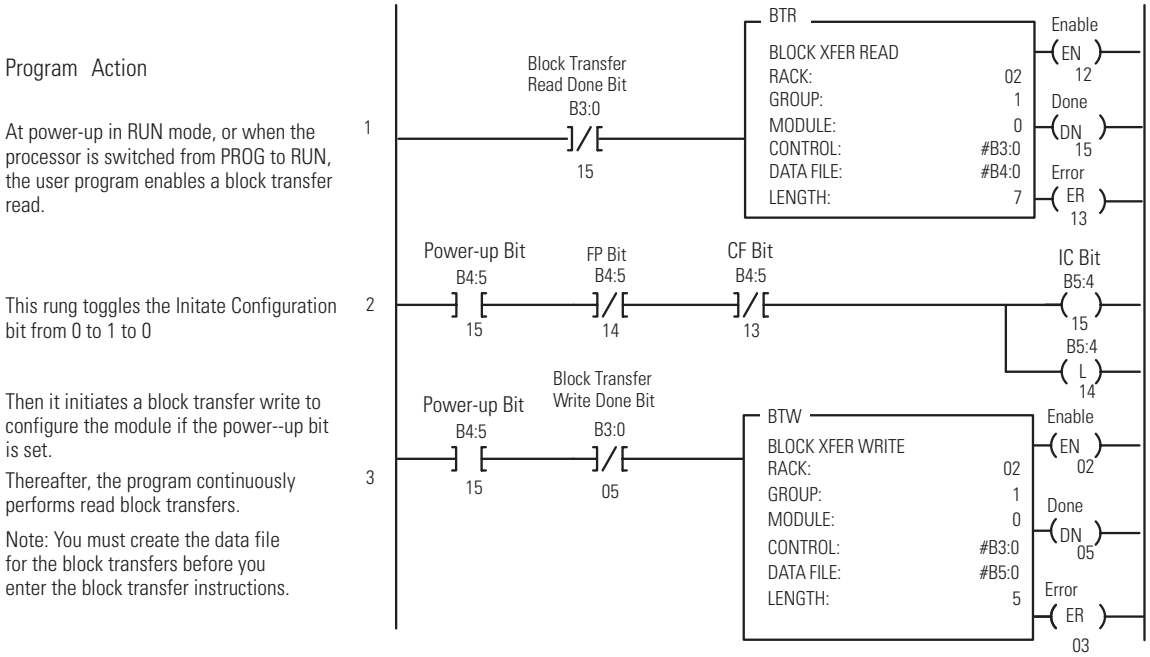


Figure 1.2
PLC-3 Family Sample Program Structure for a 1794-OF4I Module

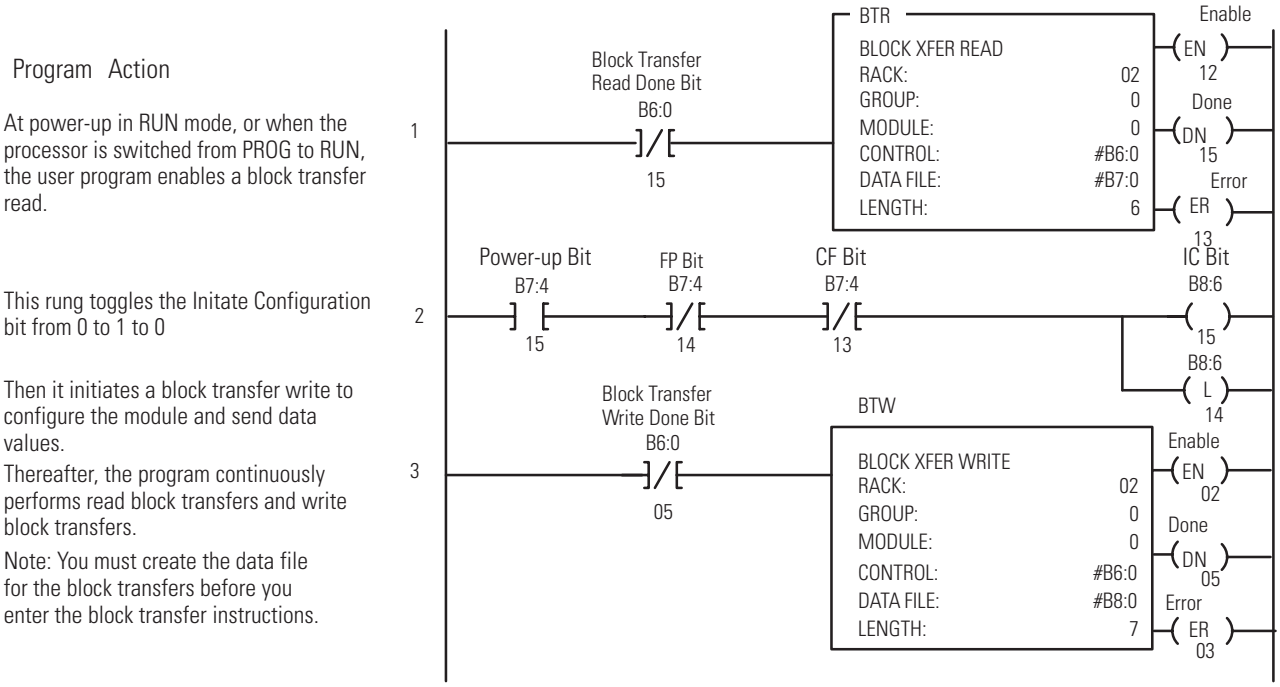


Figure 1.3
PLC-3 Family Sample Program Structure for a 1794-IF2XOF2I Module

Program Action

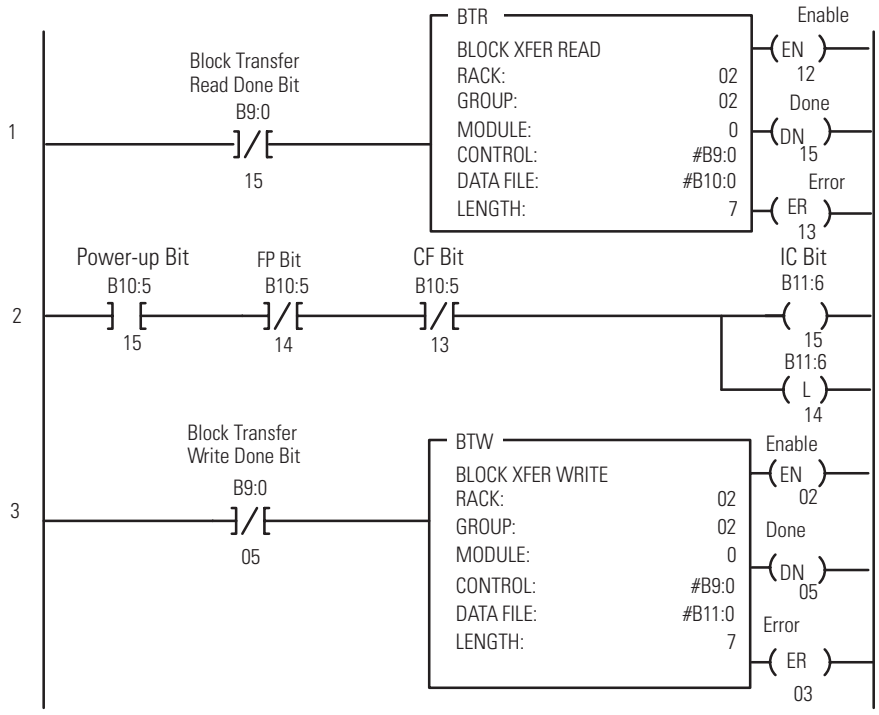
At power-up in RUN mode, or when the processor is switched from PROG to RUN, the user program enables a block transfer read.

This rung toggles the Initate Configuration bit from 0 to 1 to 0

Then it initiates a block transfer write to configure the module and send data values

Thereafter, the program continuously performs read block transfers and write block transfers.

Note: You must create the data file for the block transfers before you enter the block transfer instructions.



PLC-5 Programming

The PLC-5 program is very similar to the PLC-3 program with the following exceptions:

- block transfer enable bits are used instead of done bits as the conditions on each rung.
- separate block transfer control files are used for the block transfer instructions.

Figure 1.4
PLC-5 Family Sample Program Structure for the 1794-IF4I

Program Action

At power-up in RUN mode, or when the processor is switched from PROG to RUN, the user program enables a block transfer read.

This rung toggles the Initate Configuration bit from 0 to 1 to 0

Then it initiates a block transfer write to configure the module if the power-up bit is set.

Thereafter, the program continuously performs read block transfers to configure the module.

The pushbutton allows the user to manually request a block transfer write.

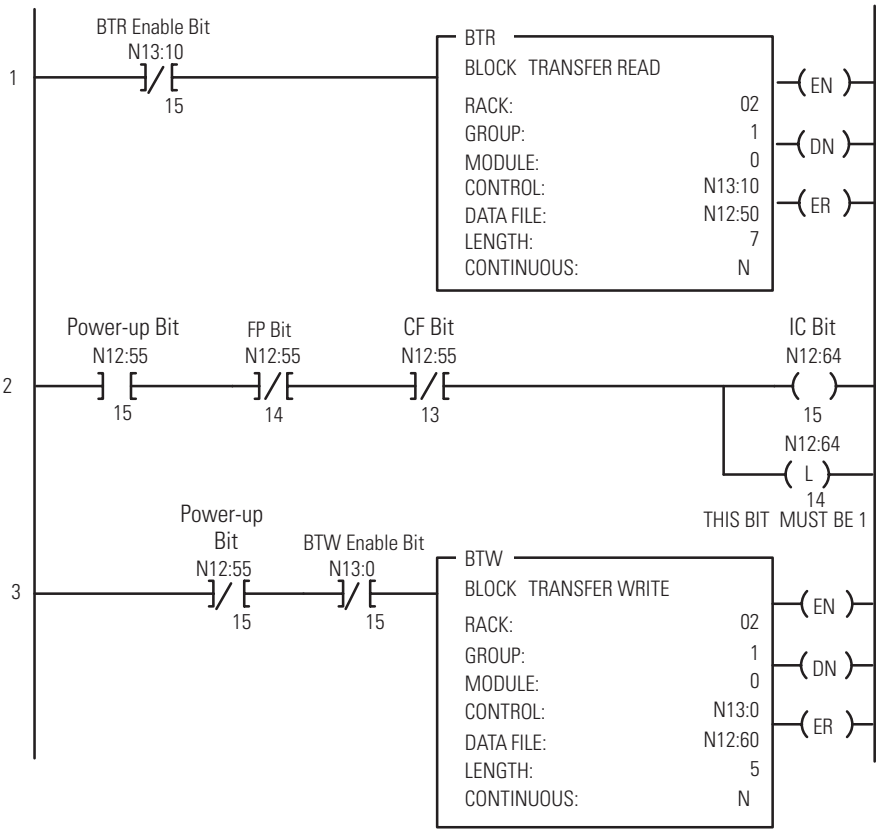


Figure 1.5
PLC-5 Family Sample Program Structure for the 1794-OF4I

Program Action

At power-up in RUN mode, or when the processor is switched from PROG to RUN, the user program enables a block transfer read.

This rung toggles the Initate Configuration bit from 0 to 1 to 0

Then it initiates a block transfer write to configure the module and send data values.

Thereafter, the program continuously performs read block transfers and write block transfers.

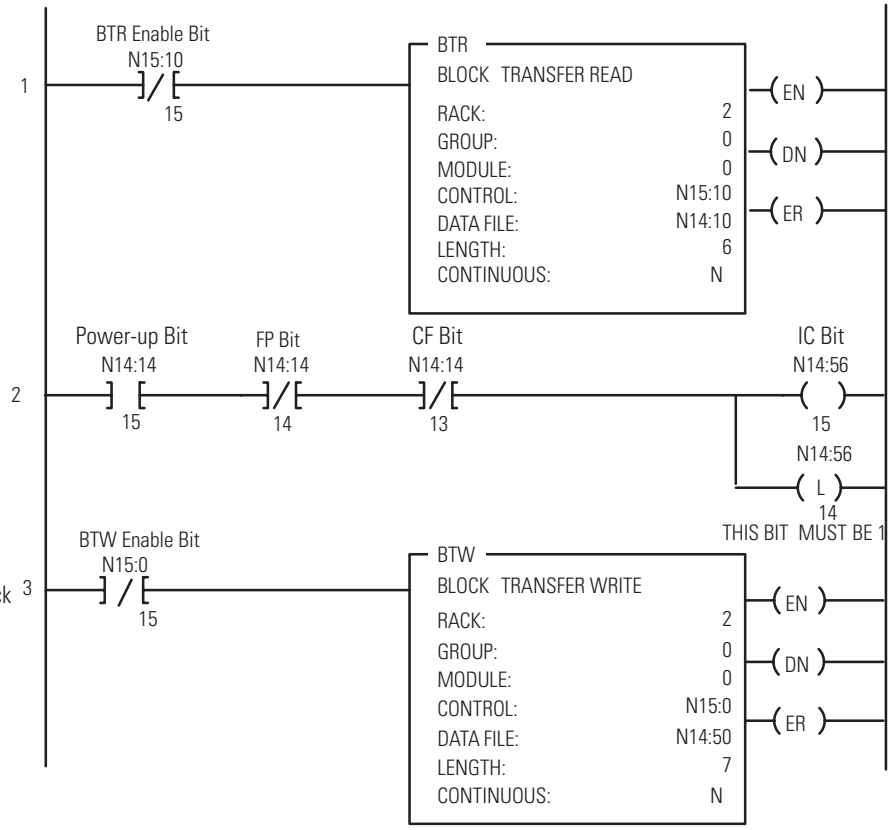


Figure 1.6
PLC-5 Family Sample Program Structure for the 1794-IF2XOF2I

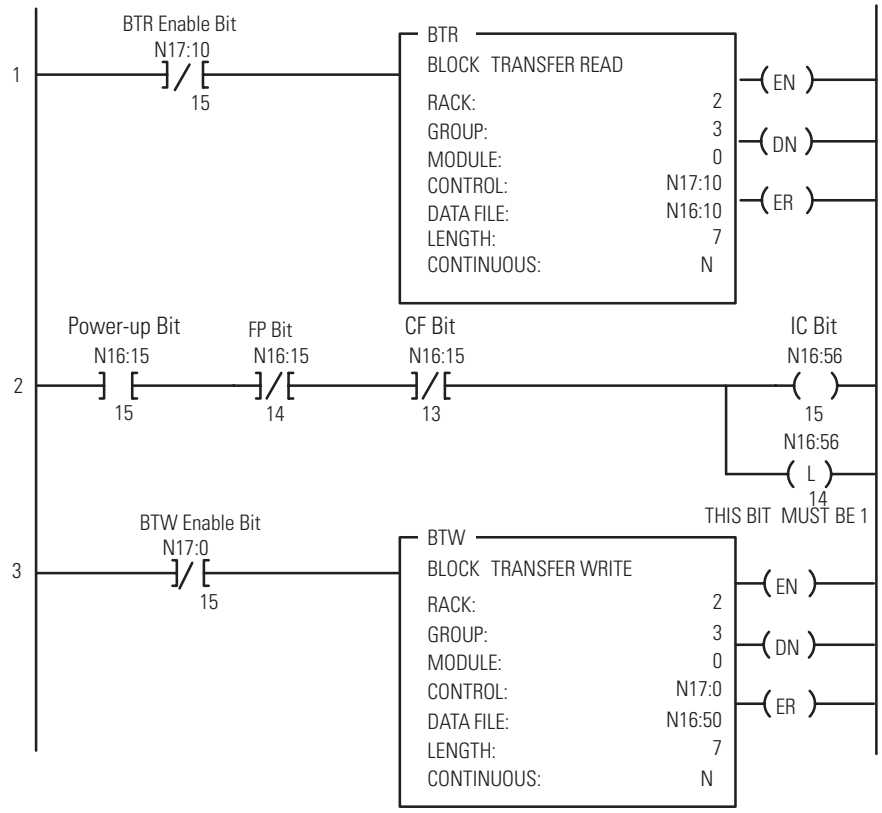
Program Action

At power-up in RUN mode, or when the processor is switched from PROG to RUN, the user program enables a block transfer read.

This rung toggles the Initate Configuration bit from 0 to 1 to 0

Then it initiates a block transfer write to configure the module and send data values.

Thereafter, the program continuously performs read block transfers and write block transfers.



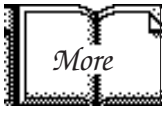
PLC-2 Programming

The 1794 analog I/O modules are not recommended for use with PLC-2 family programmable controllers due to the number of digits needed for high resolution.

SLC-5 Programming

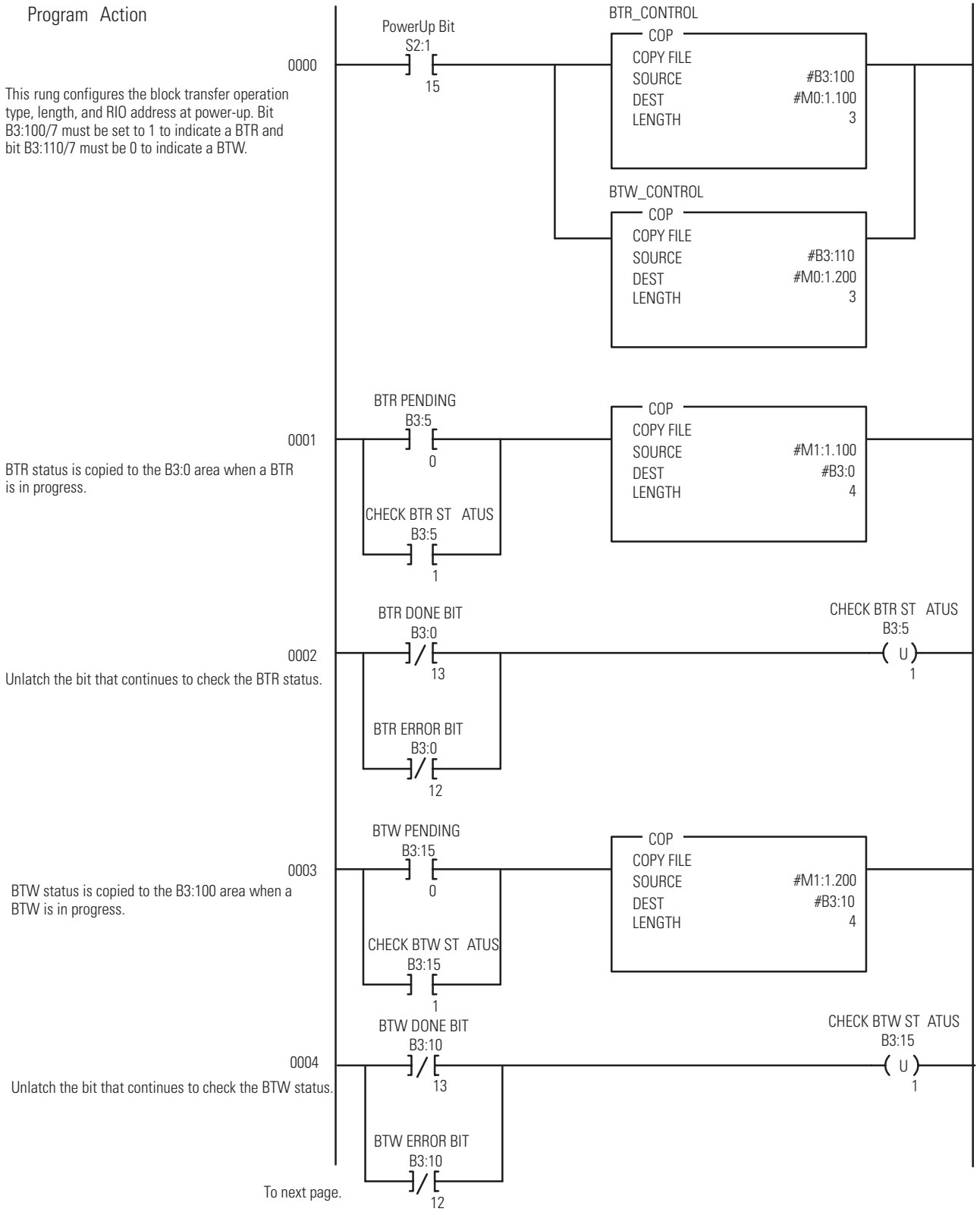
The SLC-5 programs (using the 1747-SN scanner) follow the same logic as the PLC-5 family programs in the previous examples. Differences occur in the implementation of block transfers due to the use of “M” files in the SLC system.

Configuration data for the FLEX I/O isolated analog modules and the 1747-SN scanner must be in place before executing the following programs. Chapter 4 contains information on the isolated analog module configurations.



For more information on using the 1747-SN scanner module and block transfer programming, refer to publication 1747-6.6, “Remote I/O Scanner User Manual.”

Figure 1.7
SLC Programming for the 1794-OF4I Isolated Analog Output Module

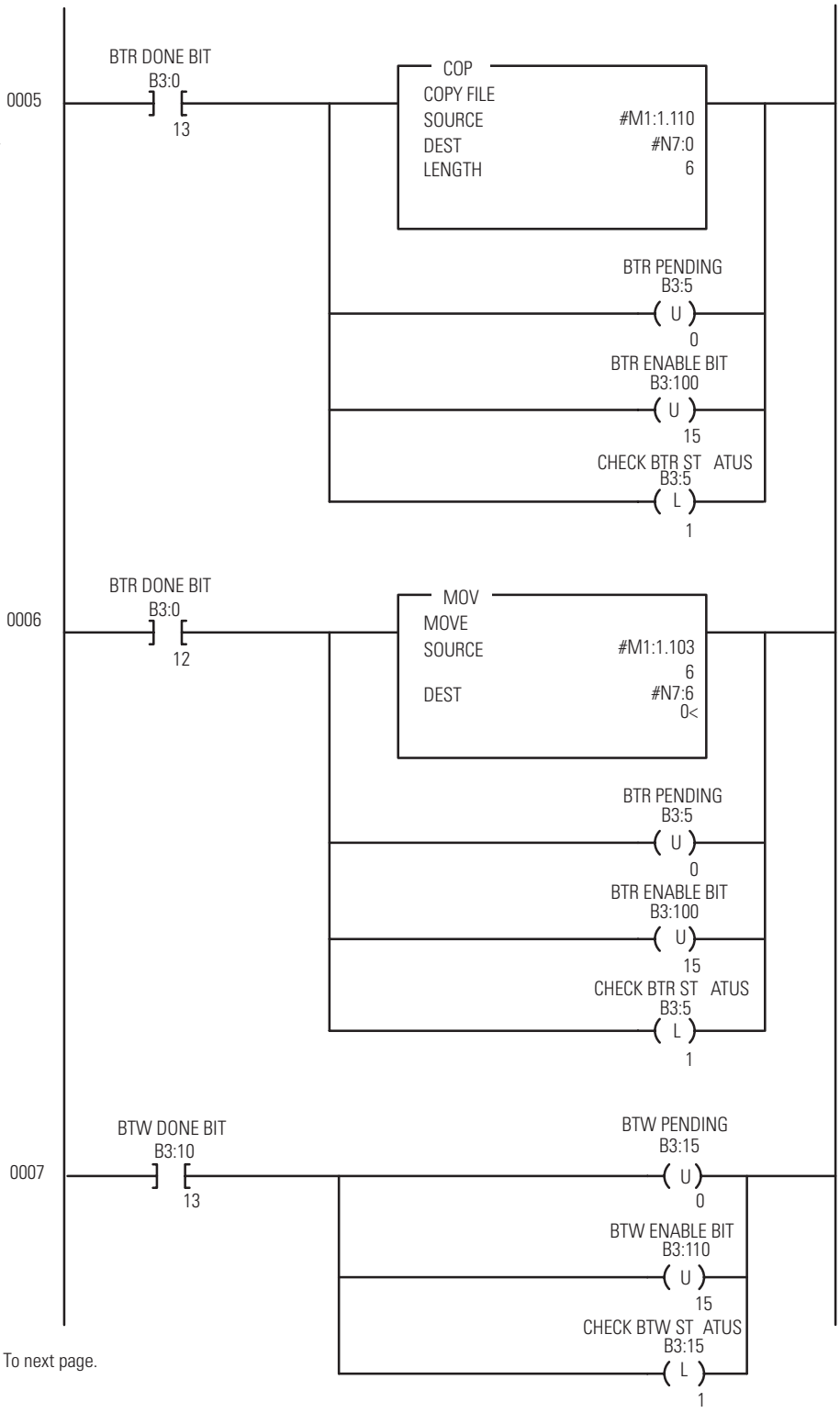


Program Action

This rung buffers the BTR data when a transfer is successfully completed.

This rung buffers the error code if a BTR is not successful.

This rung manipulates the flags for the BTW.



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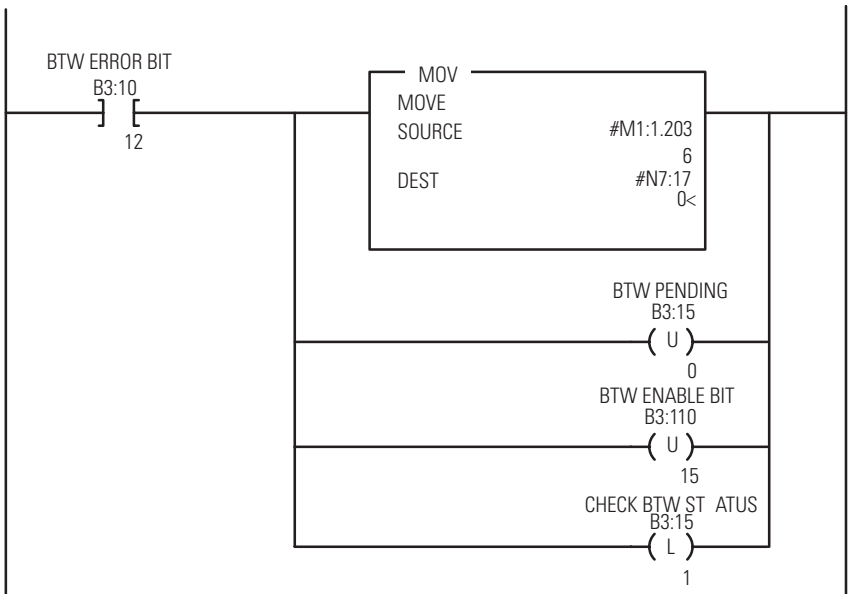
Program Action

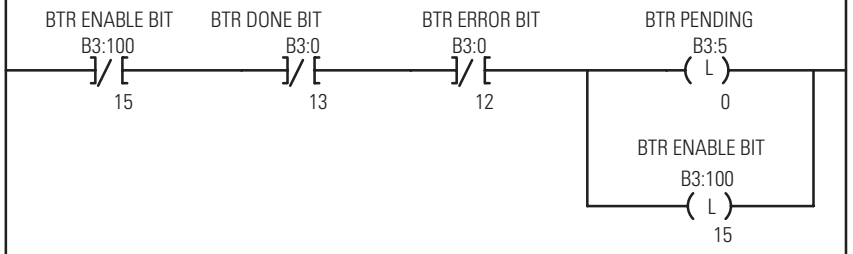
0008

This rung buffers the error code if a BTW is not successful.



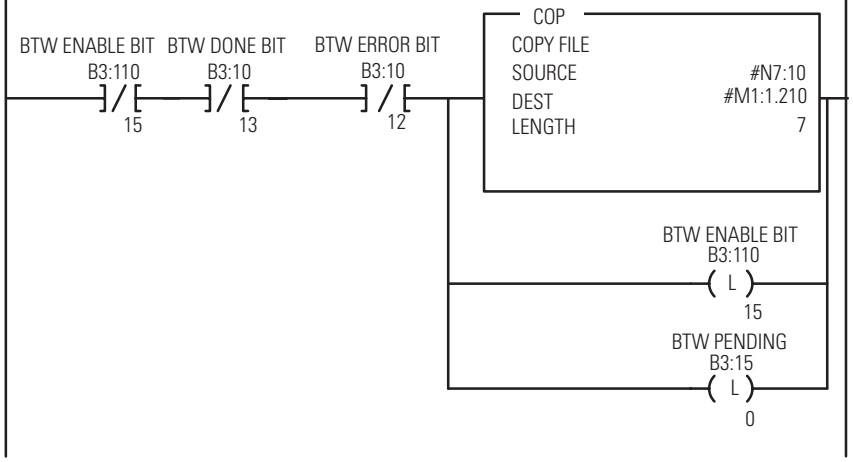
0009

This rung executes BTRs continuously .



0010

This rung copies the wirte data to the M0 file and executes BTWs continuously. The configuration data for the FLEX module should be placed in the wirte data.



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Program Action

This BTR control word is moved to the M0 file for the scanner module.

This BTW control word is moved to the M0 file for the scanner module.

This rung toggles the initiate configuration bit from 0 to 1 to 0.

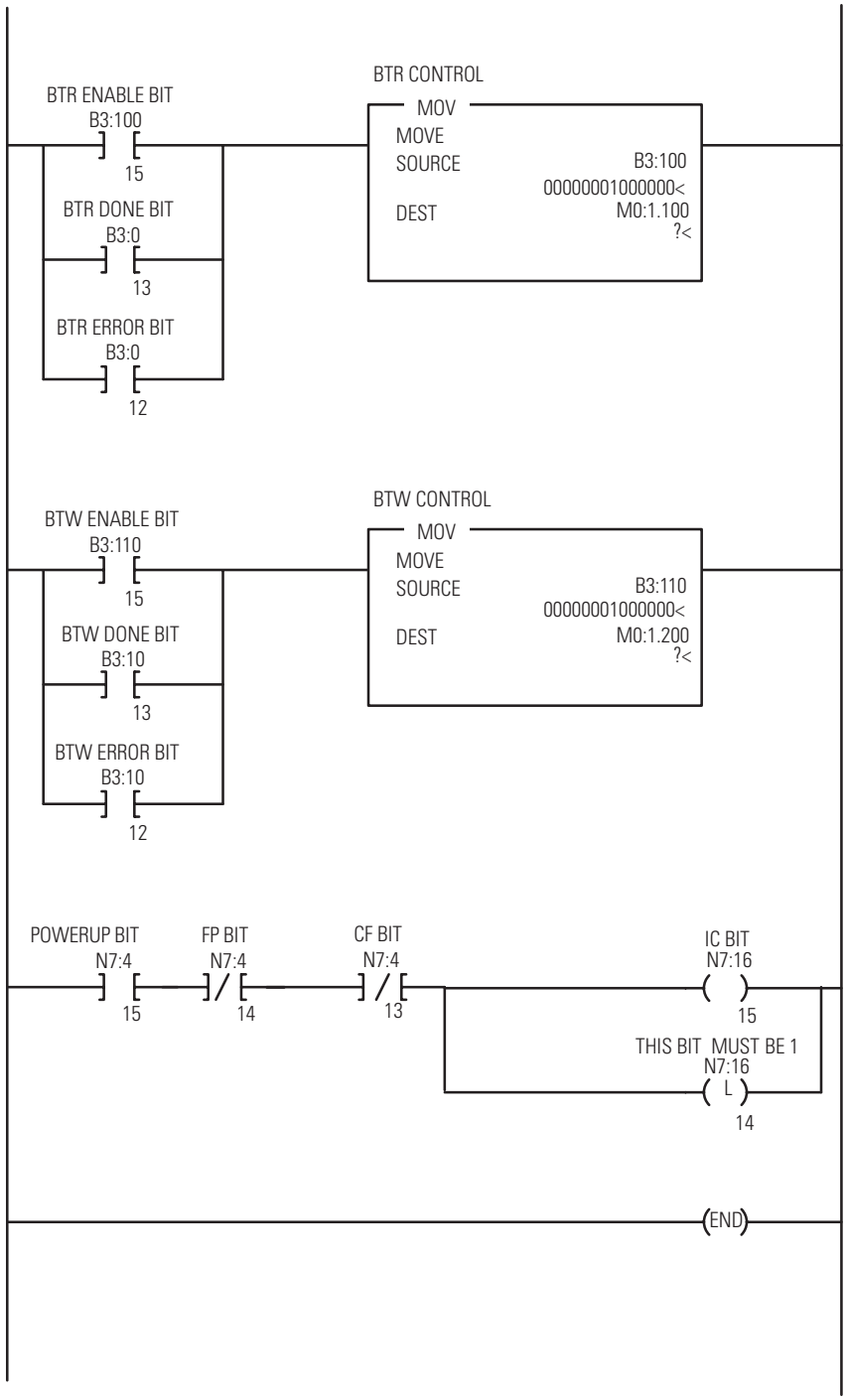
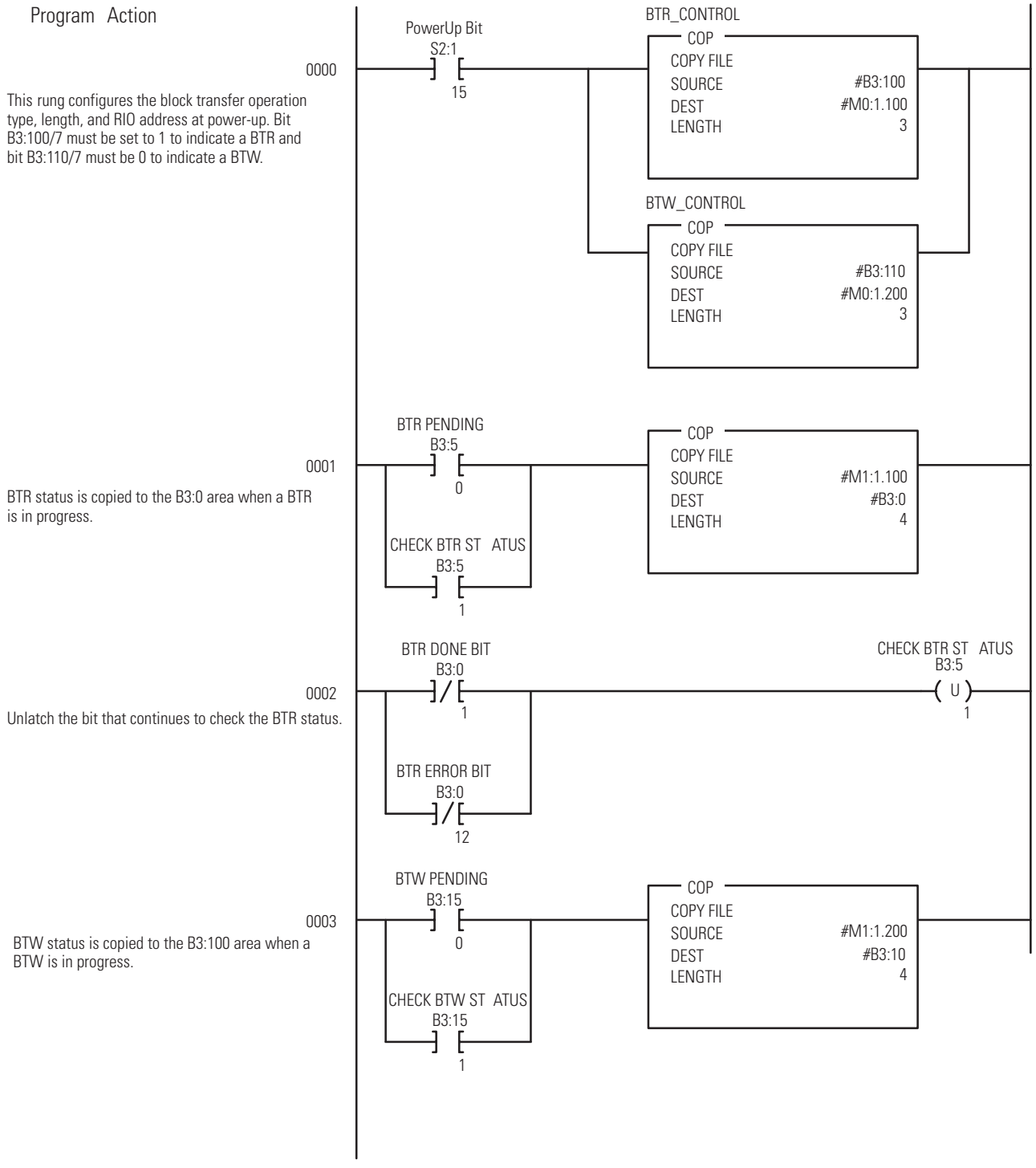


Figure 1.8
SLC Programming for the 1794-IF4I Isolated Analog Input Module

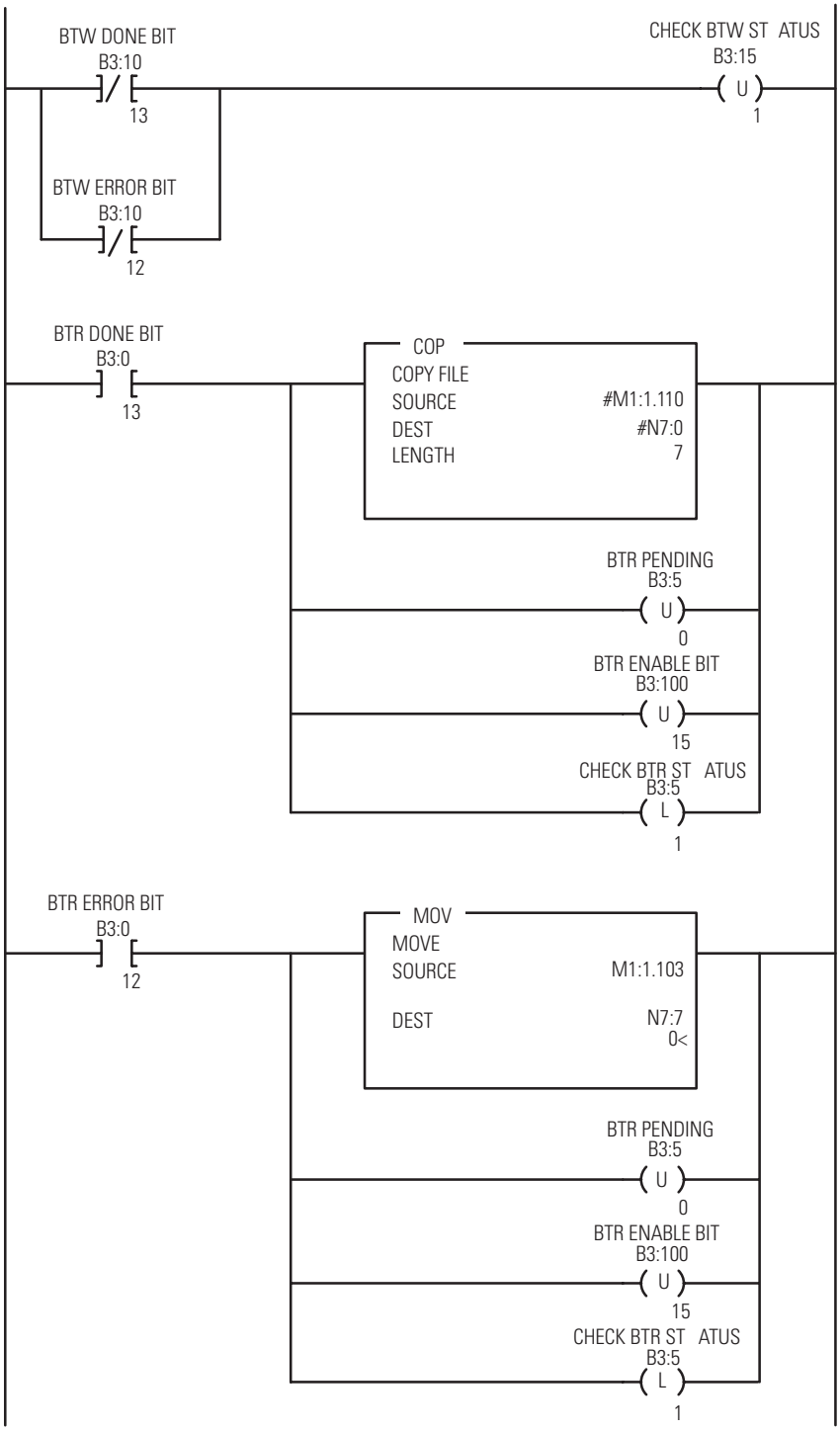


To next page.

Program Action

0004

Unlatch the bit that continues to check the BTW status.



This rung buffers the BTR data when a transfer is successfully completed.

This rung buffers the error code if a BTR is not successful.

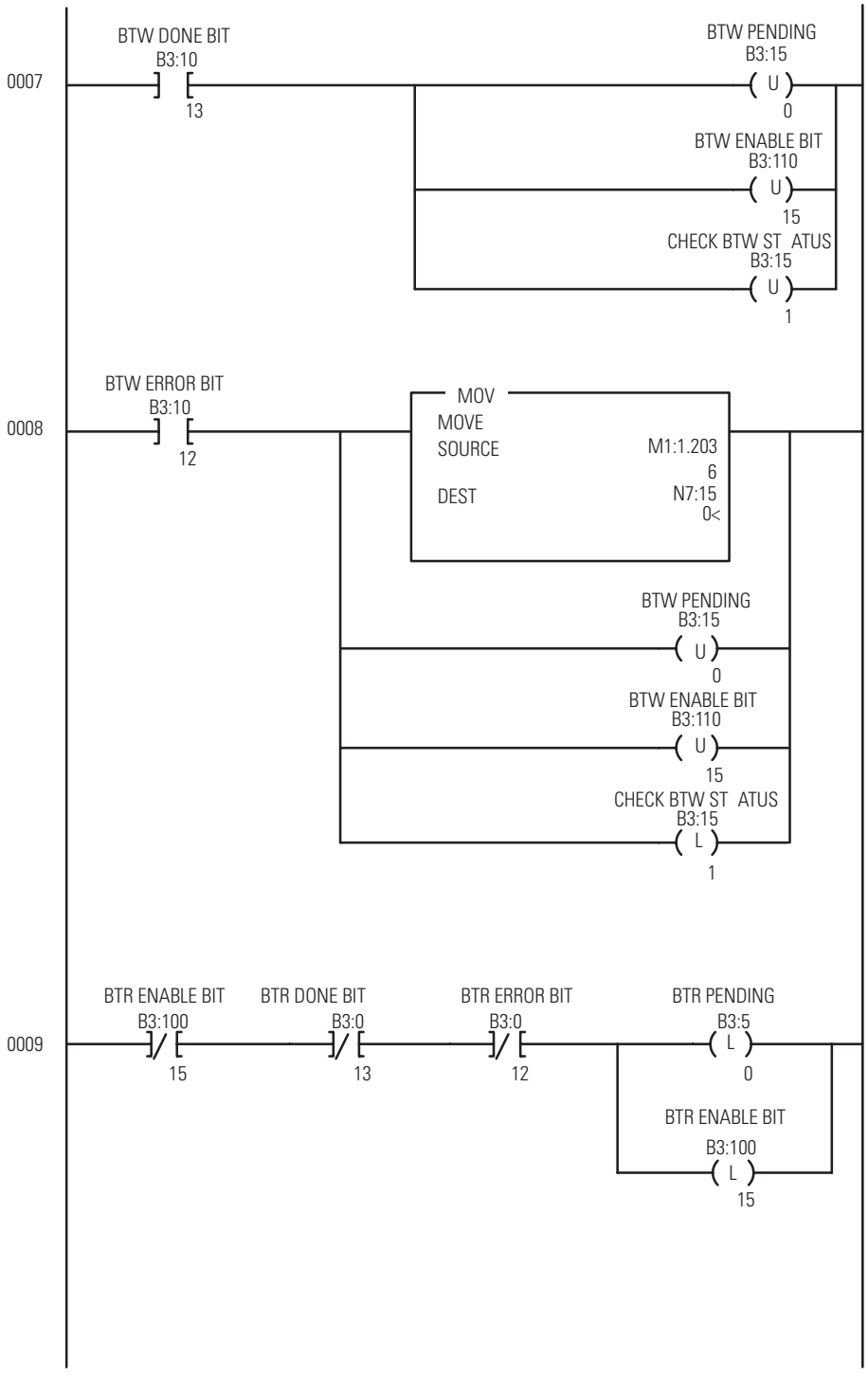
To next page.

Program Action

This rung manipulates the flags for the BTW.

This rung buffers the error code if a BTW is not successful.

This rung executes BTRs continuously .



To next page.

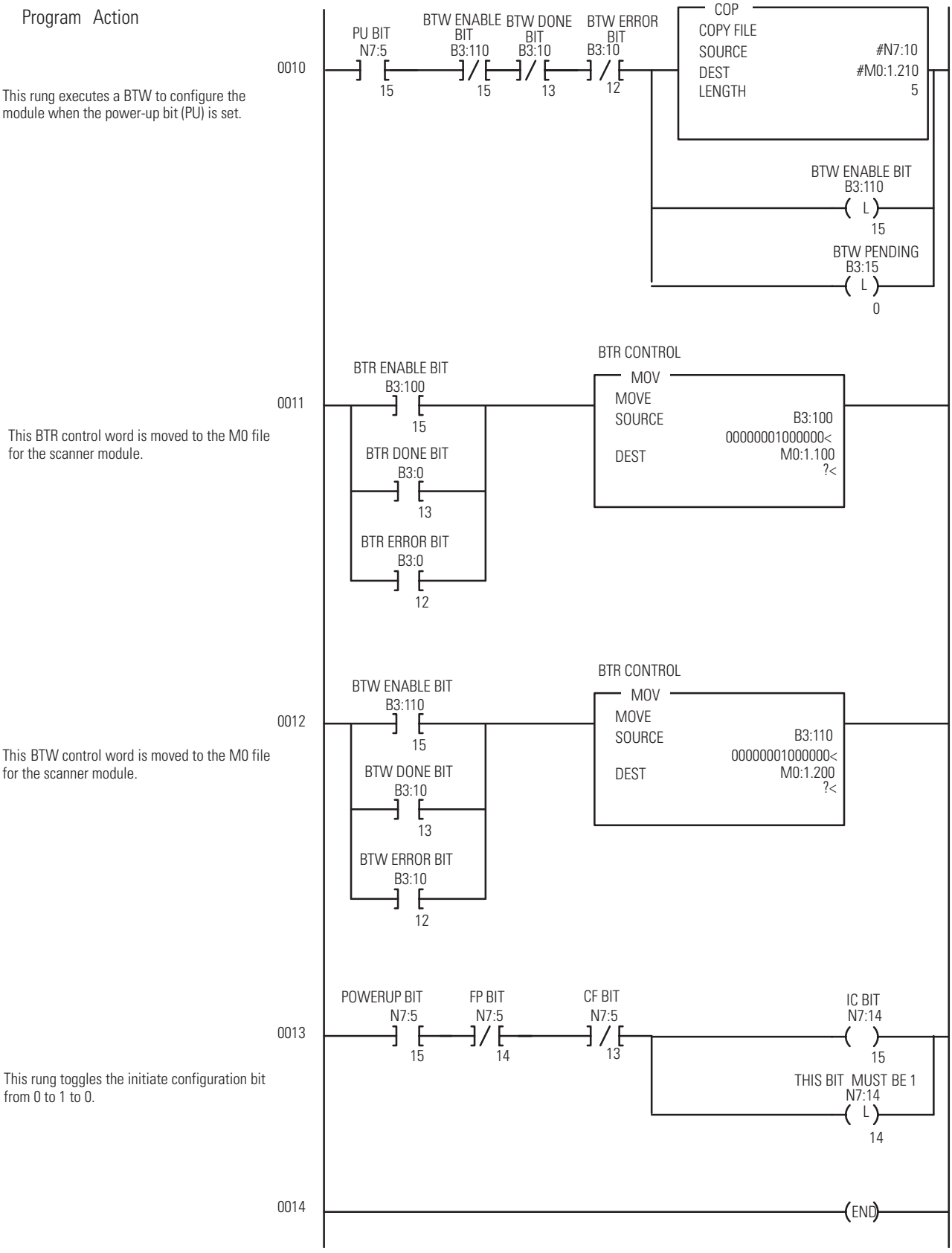
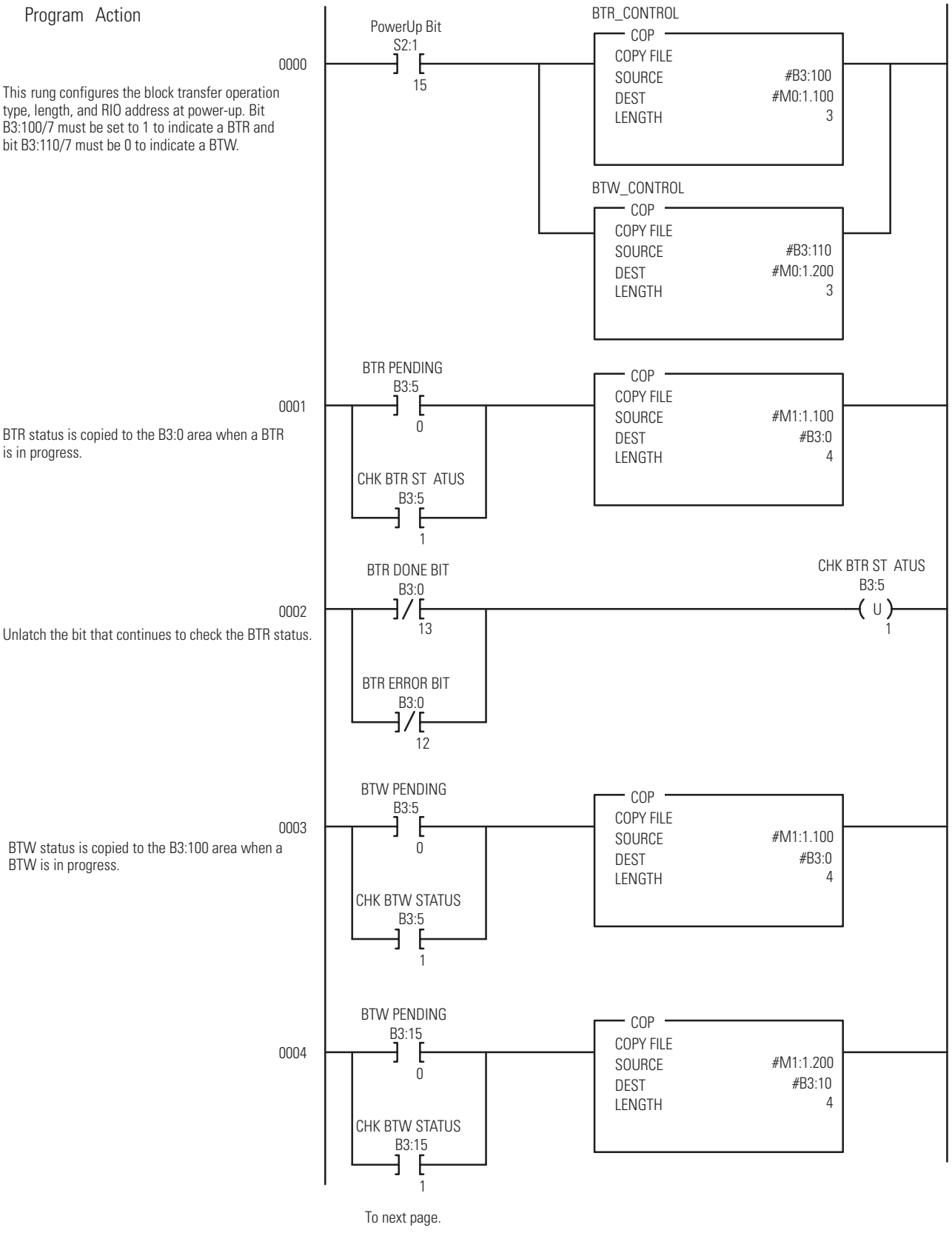
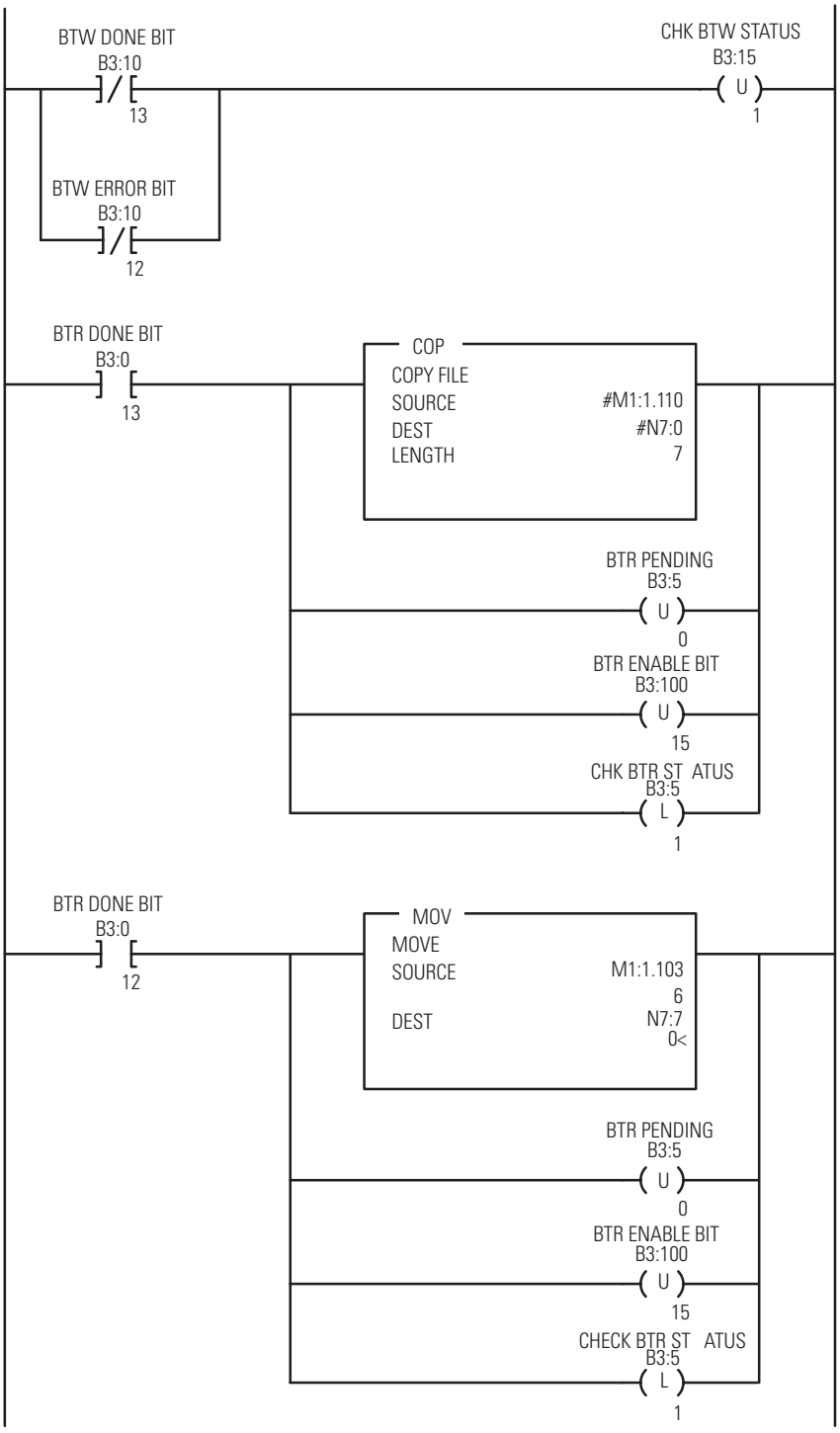

Program Action
This rung executes a BTW to configure the module when the power-up bit (PU) is set.
This BTR control word is moved to the M0 file for the scanner module.
This BTW control word is moved to the M0 file for the scanner module.
This rung toggles the initiate configuration bit from 0 to 1 to 0.
0010
PU BIT
N7:5
15
BTW ENABLE BIT
B3:110
15
BTW DONE BIT
B3:10
13
BTW ERROR BIT
B3:10
12
COP
COPY FILE
SOURCE #N7:10
DEST #M0:1.210
LENGTH 5
BTW ENABLE BIT
B3:110
L
15
BTW PENDING
B3:15
L
0
0011
BTR ENABLE BIT
B3:100
15
BTR DONE BIT
B3:0
13
BTR ERROR BIT
B3:0
12
BTR CONTROL
MOV
MOVE
SOURCE B3:100
00000001000000<
DEST M0:1.100
?<
0012
BTW ENABLE BIT
B3:110
15
BTW DONE BIT
B3:10
13
BTW ERROR BIT
B3:10
12
BTR CONTROL
MOV
MOVE
SOURCE B3:110
00000001000000<
DEST M0:1.200
?<
0013
POWERUP BIT
N7:5
15
FP BIT
N7:5
14
CF BIT
N7:5
13
IC BIT
N7:14
15
THIS BIT MUST BE 1
N7:14
L
14
0014
END

Figure 1.9
SLC Programming for the 1794-IF2XOF2I Isolated Analog Input/Output Module



Program Action



Unlatch the bit that continues to check the BTW status.

This rung buffers the BTR data when a transfer is successfully completed.

This rung buffers the error code if a BTR is not successful.

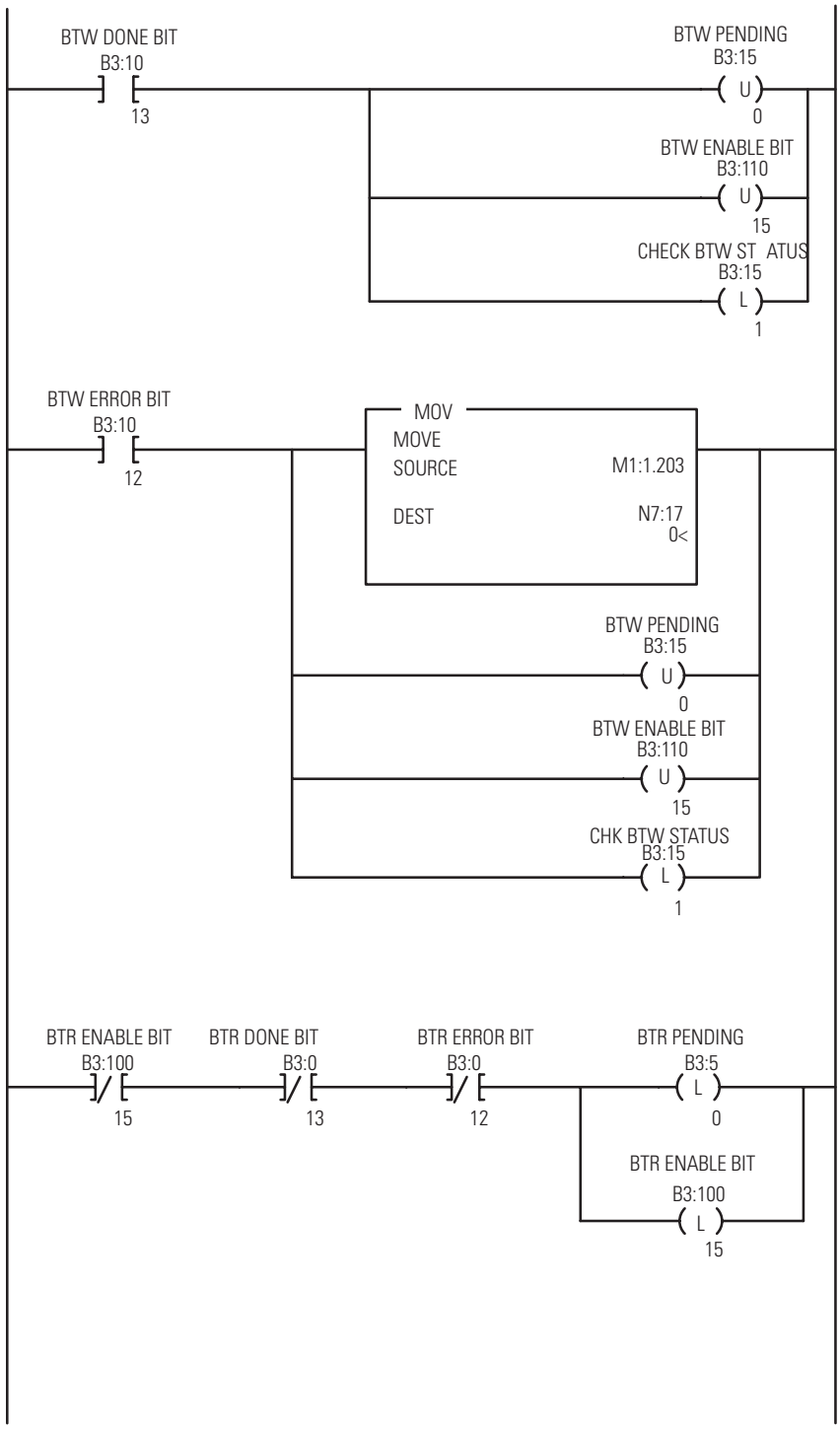
To next page.

Program Action

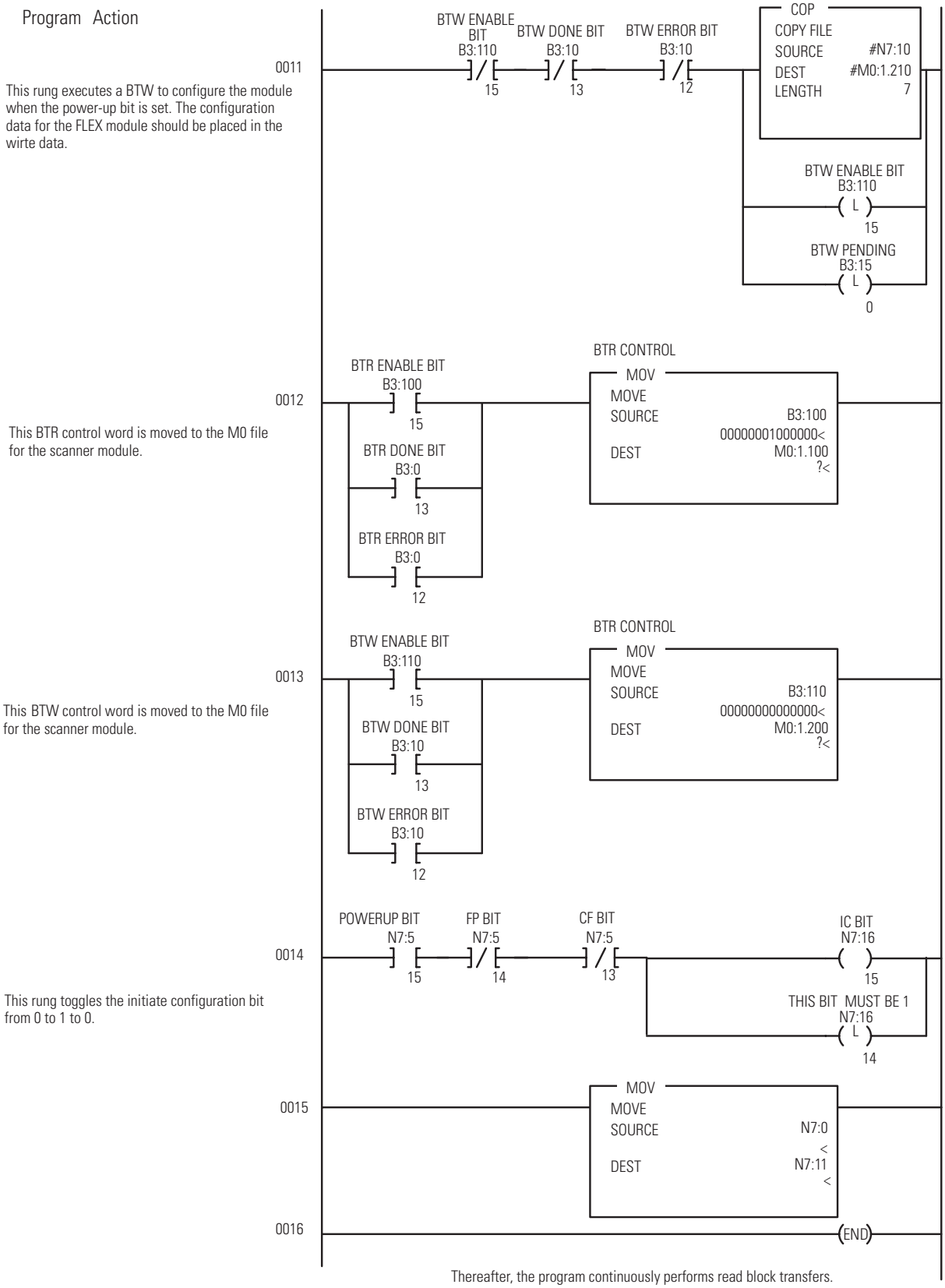
This rung manipulates the flags for the BTW.

This rung buffers the error code if a BTW is not successful.

This rung executes BTRs continuously .



To next page.


Program Action
0011
This rung executes a BTW to configure the module when the power-up bit is set. The configuration data for the FLEX module should be placed in the wirte data.
BTW ENABLE BIT B3:110 15
BTW DONE BIT B3:10 13
BTW ERROR BIT B3:10 12
COP
COPY FILE
SOURCE #N7:10
DEST #M0:1.210
LENGTH 7
BTW ENABLE BIT B3:110 L 15
BTW PENDING B3:15 L 0
0012
This BTR control word is moved to the M0 file for the scanner module.
BTR ENABLE BIT B3:100 15
BTR DONE BIT B3:0 13
BTR ERROR BIT B3:0 12
BTR CONTROL
MOV
MOVE
SOURCE B3:100
00000001000000<
DEST M0:1.100
?<
0013
This BTW control word is moved to the M0 file for the scanner module.
BTW ENABLE BIT B3:110 15
BTW DONE BIT B3:10 13
BTW ERROR BIT B3:10 12
BTR CONTROL
MOV
MOVE
SOURCE B3:110
00000000000000<
DEST M0:1.200
?<
0014
This rung toggles the initiate configuration bit from 0 to 1 to 0.
POWERUP BIT N7:5 15
FP BIT N7:5 14
CF BIT N7:5 13
IC BIT N7:16 15
THIS BIT MUST BE 1
N7:16 L 14
0015
MOV
MOVE
SOURCE N7:0
<
DEST N7:11
<
0016
END
Thereafter, the program continuously performs read block transfers.

Chapter Summary

In this chapter, you learned how to program your programmable controller. You were given sample programs for your PLC-3 and PLC-5 family processors.

Writing Configuration to and Reading Status from Your Module with a Remote I/O Adapter

Chapter Objectives

In this chapter, we tell you about:

- configuring your module's features
- entering your data
- reading data from your module
- read block format

Configuring Your Analog Module

Because of the many analog devices available and the wide variety of possible configurations, you must configure your module to conform to the analog device and specific application that you have chosen. The module is configured using a group of data table words that are transferred to the module using a block transfer write instruction.

The software configurable features available are:

- input/output range selection
- data type (two's complement, two's complement percent, binary and offset binary)

PLC-5 family programmable controllers that use 6200 software programming tools can take advantage of the IOCONFIG utility to configure these modules. IOCONFIG uses menu-based screens for configuration without having to set individual bits in particular locations. Refer to your 6200 software literature for details.

TIP RSLogix family programmable controllers that use RSLogix software programming tools can take advantage of the configuration GUI to configure these modules.

Range Selection

Individual input channels are configurable to operate with the following voltage or current ranges:

Table 4.1
Range Selection

Input channel Configuration		
Input Values	**Data Format**	**% Underrange/ % Overrange**
Channel not configured		
4–20mA	signed 2's complement	4% Under; 4% Over
±10V	signed 2's complement	2% Under, 2% Over
±5V	signed 2's complement	4% Under, 4% Over
0–20mA	signed 2's complement %	0% Under, 4% Over
4-20mA	signed 2's complement %	4% Under, 4% Over
0–10V	signed 2's complement %	0% Under, 2% Over
±10V	signed 2's complement %	2% Under, 2% Over
0–20mA	binary	0% Under, 4% Over
0–10V	binary	0% Under, 2% Over
0–5V	binary	0% Under, 4% Over
±20mA	offset binary, 8000H = 0mA	4% Under, 4% Over
4–20mA	offset binary, 8000H = 4mA	4% Under, 4% Over
±10V	offset binary, 8000H = 0V	2% Under, 2% Over
±5V	offset binary, 8000H = 0V	4% Under, 4% Over

You can select individual channel ranges using the designated words of the write block transfer instruction. Refer to the Bit/Word description for your particular module for word and bit numbers.

Safe State Selection

You can select the analog values that your output module will maintain in the event of a network communication error. When the enable bit is cleared by a communication error, the analog outputs will automatically switch to the values set in the safe state analog words as defined by the safe state source bits. This allows you to select a reset to 0V/0mA, or hold the outputs at their last state when using the remote I/O adapter on remote I/O. Additionally, safe state values can be setup using ControlNet, DeviceNet or other network adapter.

Data Format

The input/output data exchanged between the module and the adapter is available in two's complement, two's complement percent, binary and offset binary (refer to the range selection table above).

Real Time Sampling

Real time sampling (RTS) provides data gathered at precise intervals for use by the processor. You set a word in the block transfer write data file to enable RTS.

The real time sample programmed interval is the time at which updated information will be supplied to the processor. When set to "0" the module will default to each channel's fastest update rate, which is dependent on the nominal range of the input and the filter setting set to "no low pass."

When the IT interrupt toggle bit is set (1), interleaving of module interrupts occurs, ensuring exchange of critical data when channels are configured for their fastest update times. RTSI and "no low pass filter" must be 0 in order for the module to recognize this feature. This groups data update rates for all channels to the slowest configuration setting of any of the channels. In addition, channel update rates for all channels with a 7.5ms update rate are reduced to 5.0ms. When reset (0), real time sampling and filter features are enabled.

Table 4.2
Real Time Sample Interval

Configuration	Nominal Range	Channel Update Rate (RTS = 0)[1]	Channel Update Rate (RTS and Filter = 0)[1] and IT = 1
1	4-20mA	7.5ms	5.0ms
2	±10V	2.5ms	2.5ms
3	±5V	2.5ms	2.5ms
4	0-20mA	7.5ms	5.0ms
5	4-20mA	7.5ms	5.0ms
6	0-10V	5.0ms	5.0ms
7	±10V	5.0ms	5.0ms
8	0-20mA	2.5ms	2.5ms
9	4-20mA	7.5ms	5.0ms
A	0-–10V	2.5ms	2.5ms
B	0-5V	2.5ms	2.5ms
C	±20mA	2.5ms	2.5ms
D	4-20mA	7.5ms	5.0ms
E	±10V	2.5ms	2.5ms
F	±5V	2.5ms	2.5ms

(1) Channel filter set to "no low pass."

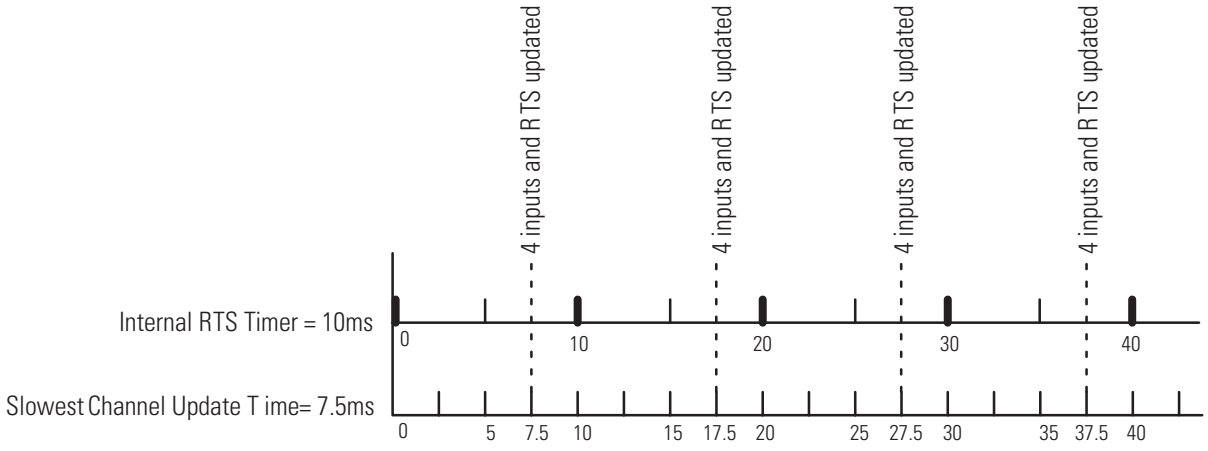
The real time sample interval can be set from 0 to 30s, in increments of 5ms. Set the real time sample interval in binary using 15 bits in the block transfer write word.

Word/Dec. Bit	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
Word/Octal Bit	**17**	**16**	**15**	**14**	**13**	**12**	**11**	**10**	**07**	**06**	**05**	**04**	**03**	**02**	**01**	**00**
Word 3	0					Real Time Sample Programmed Interval										

The individual channel update times determines how fast you can get new information collectively from the module. The module gathers the data from each input and makes it available to the processor. For example, if channel 0 is 2.5ms, channel 1 is 5.0ms, and channel 2 is 7.5ms, and RTS = 0, each channel will be updated at its stated rate. If RTS is set to 5ms, only channels 0 and 1 are fast enough to be included in the real time sample. In order to include channel 2 in your synchronous sample, you must set the RTS to 10ms minimum. Your updated information will be accurate for all inputs/outputs as viewed at the last update before the time of your request.

ATTENTION

Do not set your real time sample interval less than the slowest channel's update time.



Input Filtering

The input modules have selectable input filtering built into the A/D converter. The filter attenuates the input signal beginning at the specified frequency. You can select from 150, 300, 600, and 1200Hz with low pass filters of none, 100ms, 500ms or 1000ms. Each channel filter

can be set individually. Select the filter based on your system requirements.

A/D Conversion Rate	Low Pass Filter
1200Hz	No low pass
1200Hz	100ms low pass
1200Hz	500ms low pass
1200Hz	1000ms low pass
600Hz	No low pass
600Hz	100ms low pass
600Hz	500ms low pass
600Hz	1000ms low pass
300Hz	No low pass
300Hz	100ms low pass
300Hz	500ms low pass
300Hz	1000ms low pass
150Hz	No low pass
150Hz	100ms low pass
150Hz	500ms low pass
150Hz	1000ms low pass

Reading Data From Your Module

Read programming moves status and data from the module to the processor's data table. The processor's user program initiates the request to transfer data from the input module (or combination module) to the processor.

Mapping Data for the Analog Modules

The following read and write words and bit/word descriptions describe the information written to and read from the analog modules. Each word is composed of 16 bits.

8 Input Analog Module (Cat. No. 1794-IF4I)

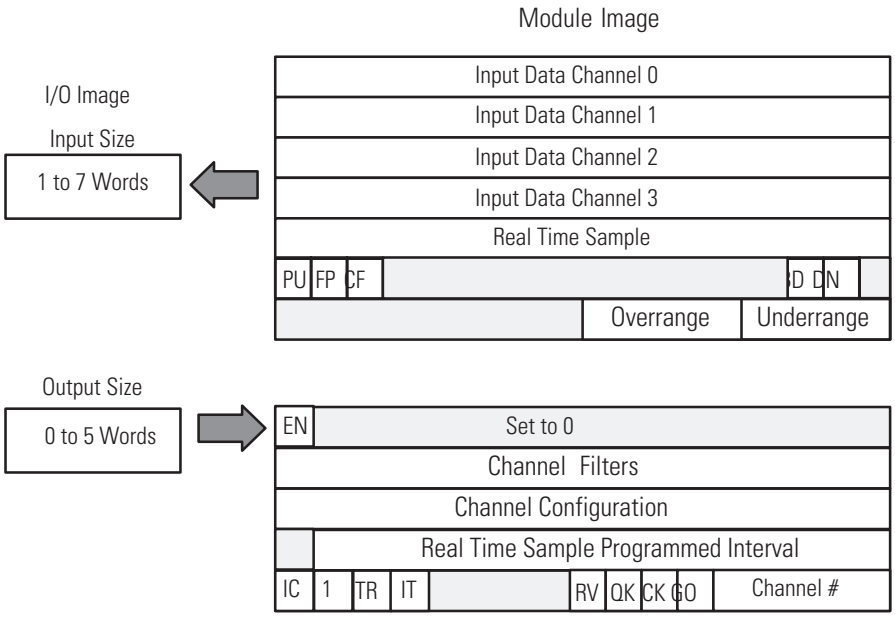


Table 4.3
Analog Input Module (1794-IF4I) Read

Word/Dec. Bit	**15**	**14**	**13**	**12**	**11**	**10**	**09**	**08**	**07**	**06**	**05**	**04**	**03**	**02**	**01**	**00**
Word/Octal Bit	**17**	**16**	**15**	**14**	**13**	**12**	**11**	**10**	**07**	**06**	**05**	**04**	**03**	**02**	**01**	**00**
Read Word 0	Analog Value Channel 0															
Word 1	Analog Value Channel 1															
Word 2	Analog Value Channel 2															
Word 3	Analog Value Channel 3															
Word 4	Real Time Sample															
Word 5	PU	FP	CF	0		Reserved			0	0	0	0	0	BD	DN	0
Word 6	0	0	0	0	0	0	0	0	V3	V2	V1	V0	U3	U2	U1	U0

Where:
PU = Power up unconfigured state
FP = Field power off
CF = In configuration mode
BD = Calibration bad
DN = Calibration accepted
U = Under range for specified channel
V = Overrange for specified channel

Table 4.4
Word/Bit Descriptions for the 1794-IF4I Analog Input Module

Read Word	Decimal Bit (Octal Bit)	Definition
Word 0	Bits 00-15 (00-17)	**Channel 0 analog data** – Real time input data per your configuration
Word 1	Bits 00-15 (00-17)	**Channel 1 analog data** – Real time input data per your configuration
Word 2	Bits 00-15 (00-17)	**Channel 2 analog data** – Real time input data per your configuration
Word 3	Bits 00-15 (00-17)	**Channel 3 analog data** – Real time input data per your configuration
Word 4	Bits 00-15 (00-17)	**Real Time Sample**. The elapsed time in increments programmed by the real time sample interval.
Word 5	Bits 00	Reserved
	Bits 01	**Calibration Done bit (DN). –** This bit is set to 1 after a calibration cycle is
	Bits 02	**Calibration Bad bit (BD). –** This bit is set to 1 if the channel calibration
	Bits 03–07	Set to 0.
	Bits 08–11 (10-12)	Reserved
	Bit 12 (14)	Set to 0
	Bit 13 (15)	**Configuration mode bit (CF)** – This bit is set (1) when the calibration mode is selected (bit 15, word 5 in the block transfer write set to 1). When this bit is set (1), the module status indicator flashes.
	Bit 14 (16)	**Field Power Off bit (FP)** – This bit is set (1) when the 24V field power fails. When this bit is set (1), the module status indicator flashes.
	Bit 15 (17)	**Power Up (unconfigured state) bit (PU).** – This bit is set (1) when the configuration word is all zeroes (0) due to a reset (adapter power cycle or module insertion) or a cleared configuration word (all 0). When this bit is set (1), the module status indicator flashes.
Word 6	Bits 00-03	**Underrange bits (U). –** These bits are set (1) when the input channel is below a preset limit as defined by the configuration selected. U0 (bit 00) corresponds to input channel 0 and U1 (bit 01) corresponds to input channel 1, etc. Refer to Table 4.B.
	Bits 04-07	**Overrange bits (V).** – These bits are set (1) when the input channel is above a preset limit as defined by the configuration selected. Bit 04 corresponds to input channel 0 and bit 05 corresponds to input channel 1, etc. Refer to Table 4.8.
	Bits 08–15 (10-17)	Not used. Set to 0.

Table 4.5
Analog Input Module (1794-IF4I) Write Configuration Block

Word/Dec. Bit	**15**	**14**	**13**	**12**	**11**	**10**	**09**	**08**	**07**	**06**	**05**	**04**	**03**	**02**	**01**	**00**
Word/Octal Bit	**17**	**16**	**15**	**14**	**13**	**12**	**11**	**10**	**07**	**06**	**05**	**04**	**03**	**02**	**01**	**00**
Word 0	EN	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Word 1	Chnl 3 Filter				Chnl 2 Filter				Chnl 1 Filter				Chnl 0 Filter			
Word 2	Chnl 3 Configuration				Chnl 2 Configuration				Chnl 1 Configuration				Chnl 0 Configuration			
Word 3	0	Real Time Sample Programmed Interval														
Word 4	IC	1	TR	IT	0	0	0	0	RV	QK	CK	GO	Channel Number			

Where:
EN = Not used on the 1794-IF4I.
IC = Initiate configuration bit
TR = Transparent bit
IT = Interrupt Toggle bit
RV = Revert to defaults bit
QK = Quick calibration
CK = Calibration clock
GO = Gain offset select

Table 4.6
Word/Bit Descriptions for the 1794-IF4I Analog Input ModuleWrite

Write Word	**Decimal Bit (Octal Bit)**	**Definition**
Word 0	Bits 00–14 (00–16)	Not used. Set to 0.
	Bit 15 (17)	**Output enable bit (EN).** – Not used in the 1794-IF4I module.
Word 1	Channels 0 through 3 Filter Selections (refer to Table 4.7)	
	Bits 00–03	Channel 0 Filter Setting
	Bits 04–07	Channel 1 Filter Setting
	Bits 08–11 (10–13)	Channel 2 Filter Setting
	Bits 12–15 (14–17)	Channel 3 Filter Setting
Word 2	Channel Configuration (refer to Table 4.B)	
	Bits 00–03	Channel 0 Configuration
	Bits 04–07	Channel 1 Configuration
	Bits 08–11 (10–13)	Channel 2 Configuration
	Bits 12–15 (14–17)	Channel 3 Configuration
Word 3	Bits 00–14 (00–16)	**Real Time Sample Interval –** Programs the interval of the real time sample. Can be varied from 0 to 30 seconds (30000 decimal). Resolution is in ms with granularity in 5ms steps.
	Bit 15 (17)	Not used. Set to 0.

Table 4.6
Word/Bit Descriptions for the 1794-IF4I Analog Input ModuleWrite

Write Word	Decimal Bit (Octal Bit)	Definition
Word 4	Bit 00–03	**Channel calibration selection bit.** When this bit is set (1), the channel can be calibrated using the calibration clock bit (CK). Bit 00 corresponds to input channel 0, bit 01 corresponds to input channel 1, it 02 corresponds to input channel 2, bit 03 corresponds to input channel 3
	Bit 04	**Gain/Offset selection bit (GO).** – When this bit is cleared, a 0 to 1 to 0 transition of the CK bit performs on offset calibration. When this bit is 1, the module is directed to do a gain calibration.
	Bit 05	**Calibration clock bit (CK). –** When this bit is set to 1 (calibration mode), the calibration coeffiicient for the selected channels is accepted. When this bit is reset (0), the accepted calibration coefficients for the selected channels are stored, applied, and the calibration mode exited. Monitor status bits DN and BD for succesful calibration.
	Bit 06	**Quick Calibration bit (QK).** – Normally reset (0). When this bit is set (1) during a calibration sequence, the calibration coefficient is stored to all related configurations for the selected channels. **NOTE:** This method of calibration quickly calibrates the selected channels, however you will not be within the rated accuracy of the module.
	Bit 07	**Revert to defaults bit (RV).** – Normally reset (0). When set (1) during a calibration procedure, default values for selected channels are used for the calibration coefficient.**NOTE:** You will not be within the rated accuracy of the module.
	Bits 08-11 (10-13)	Not used. Set to 0. For IF4ICFXT only: Bit 8 — **FastStepResponse (FR)** forces the A/D to skip the FIR stage if an input step occurs. An averaging algorithm is temporarily used instead of the FIR filter in the A/D to provide a quicker response. Bit 9 — **FIRFilterDisable (SK)** bypasses the FIR filter stage in the A/D. Bit 10 — **ChopModeDisable (CH)** disables the chop mode in the A/D. Chop mode is used to reduce offsets between input and output of the analog section of the A/D. (1) **Note:** Module level settings that only affect 150 Hz, 300 Hz, and 600 Hz conversion rate settings.
	Bit 12 (14)	**Interrupt Toggle bit (IT)** – This bit, when set (1), permits interleaving of module interrupts ensuring exchange of critical data when channels are configured for their fastest update times. RTSI and "no low pass filter" must be 0 in order for the module to recognize this feature. This groups data update rates for all channels to the slowest configuration setting of any of the channels. In addition, channel update rates for all channels with a 7.5ms update rate are reduced to 5.0ms. When reset (0), real time sampling and filter features are enabled.
	Bit 13 (15)	**Transparent bit (TR).** – This bit, when set to 1, permits configuration to be changed without using the IC bit. Default setting for this bit is True (1)
	Bit 14 (16)	Always set to 1.
	Bit 15 (17)	**Initiate Configuration bit (IC).** – When set (1), instructs the module to enter configuration mode. Present configuration data prior to or coincident with IC being set. Once IC returns to 0, the configuration is applied and any subquent configuration information is ignored until IC is toggled.

(1) For changes in tag values like the CH bit in the IF4ICFXT to take effect, the tag either must be included in a ladder rung or or a configuration download forced using the configuration tab in the RSLogix GUI.

Table 4.7
Setting the Input Filter

Bits				Channel	
03	02	01	00	Input 0	
07	06	05	04	Input 1	
11	10	09	08	Input 2	
15	14	13	12	Input 3	
				A/D Conversion Rate	**Low Pass Filter**
0	0	0	0	1200Hz	No low pass
0	0	0	1	1200Hz	100ms low pass
0	0	1	0	1200Hz	500ms low pass
0	0	1	1	1200Hz	1000ms low pass
0	1	0	0	600Hz	No low pass
0	1	0	1	600Hz	100ms low pass
0	1	1	0	600Hz	500ms low pass
0	1	1	1	600Hz	1000ms low pass
1	0	0	0	300Hz	No low pass
1	0	0	1	300Hz	100ms low pass
1	0	1	0	300Hz	500ms low pass
1	0	1	1	300Hz	1000ms low pass
1	1	0	0	150Hz	No low pass
1	1	0	1	150Hz	100ms low pass
1	1	1	0	150Hz	500ms low pass
1	1	1	1	150Hz	1000ms low pass

Table 4.8
Configuring Your Input Module

Input Channel Configuration				
03	02	01	00	Set these bits for Channel 0
07	06	05	04	Set these bits for Channel 1
11	10	09	08	Set these bits for Channel 2
15	14	13	12	Set these bits for Channel 3

Table 4.8
Configuring Your Input Module

Bit Settings				Input Values	Data Format	% Underrange %Overrange	Input Range[2]		Module Update Rate	
							Hexadecimal	Decimal	(RTSI = 0)	(RTSI = 0) IT = 1
0	0	0	0	Channel not configured						
0	0	0	1	4–20mA	signed 2's complement	4% Under; 4% Over	<0000–7878>	<0000–30840>	7.5ms	5.0ms
0	0	1	0	±10V	signed 2's complement	2% Under, 2% Over	<831F–7CE1>	<–31969–31969>	2.5ms	2.5ms
0	0	1	1	±5V	signed 2's complement	4% Under, 4% Over	<8618–79E8>	<–31208–31208>	2.5ms	2.5ms
0	1	0	0	0–20mA	signed 2's complement %	0% Under, 4% Over	0–2710>	0–10000>	7.5ms	5.0ms
0	1	0	1	4-20mA	signed 2's complement %	4% Under, 4% Over	<0–2710>	<0–10000>	7.5ms	5.0ms
0	1	1	0	0–10V	signed 2's complement %	0% Under, 2% Over	0–2710>	0–10000>	5.0ms	5.0ms
0	1	1	1	±10V	signed 2's complement %	2% Under, 2% Over	<–D8F0–2710>	<–10000–10000>	5.0ms	5.0ms
1	0	0	0	0–20mA	binary	0% Under, 4% Over	0000–F3CF>	0000–62415>	2.5ms	2.5ms
1	0	0	1	4–20mA[1]	binary	4% Under, 4% Over	0000–F0F1>	0000–61681>	7.5ms	5.0ms
1	0	1	0	0–10V	binary	0% Under, 2% Over	0000–F9C2>	0000–63938>	2.5ms	2.5ms
1	0	1	1	0–5V	binary	0% Under, 4% Over	0000–F3CF>	0000–62415>	2.5ms	2.5ms
1	1	0	0	±20mA	offset binary, 8000H = 0mA	4% Under, 4% Over	<0618–F9E8>	<1560–63976>	2.5ms	2.5ms
1	1	0	1	4–20mA	offset binary, 8000H = 4mA	4% Under, 4% Over	<8000–F878>	<32768–63608>	7.5ms	5.0ms
1	1	1	0	±10V	offset binary, 8000H = 0V	2% Under, 2% Over	<031F–FCE1>	<799–64737>	2.5ms	2.5ms
1	1	1	1	±5V	offset binary, 8000H = 0V	4% Under, 4% Over	<0618–F9E8>	<1560–63976>	2.5ms	2.5ms

(1) Underrange for 4-20mA occurs in the blind area below 0 (3.2mA).

(2) < and > indicate the overrun beyond actual range (about 5%).

4 Isolated Output Analog Module (Cat. No. 1794-OF4I)

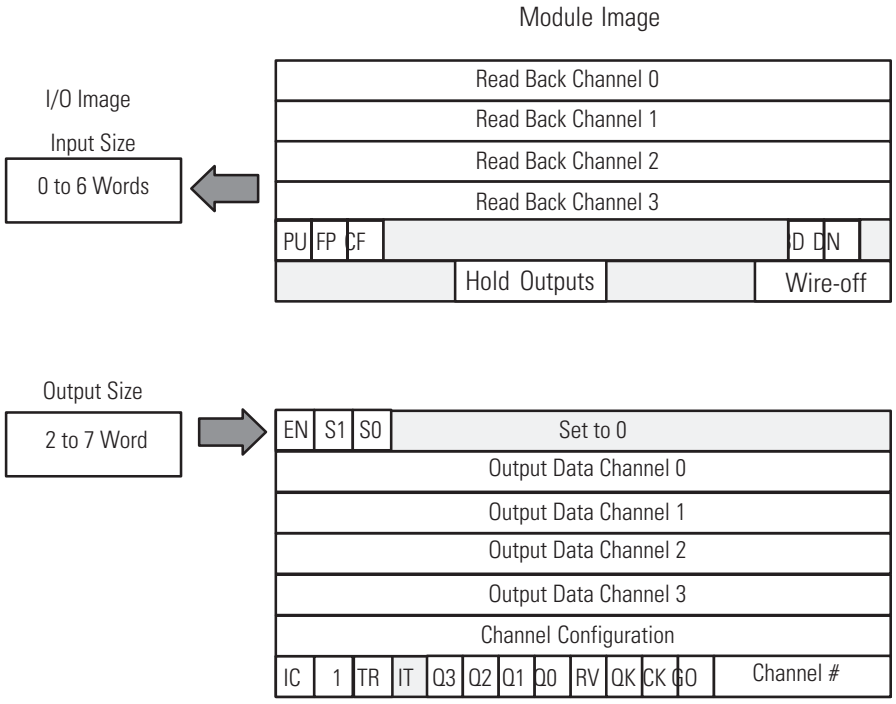


Table 4.9
Analog Output Module (1794-OF4I) Read

Word/Dec. Bit	**15**	**14**	**13**	**12**	**11**	**10**	**09**	**08**	**07**	**06**	**05**	**04**	**03**	**02**	**01**	**00**
Word/Octal Bit	**17**	**16**	**15**	**14**	**13**	**12**	**11**	**10**	**07**	**06**	**05**	**04**	**03**	**02**	**01**	**00**
Read Word 0	Read Back Channel 0															
Word 1	Read Back Channel 1															
Word 2	Read Back Channel 2															
Word 3	Read Back Channel 3															
Word 4	PU	FP	CF	0	Reserved				0	0	0	0	0	BD	DN	0
Word 5	0	0	0	0	P3	P2	P1	P0	0	0	0	0	W3	W2	W1	W0

Where:
PU = Power up unconfigured state
FP = Field power off
CF = In configuration mode
BD = Calibration bad
DN = Calibration accepted
P0 thru P3 = Output holding in response to Q0 thru Q3
W0 thru W3 = Wire off current loop status for channels 0 thru 3 respectively. (Not used on voltage outputs.)

Table 4.10
Bit/Word Descriptions for the 1794-OF4I Analog Output Module Read

Read Word	Decimal Bit (Octal Bit)	Definition
Word 0	Bits 00-15 (00-17)	**Read Back Channel 0** – During normal operation, it is a copy of the output of channel 0. During an EN transition, it is the condition of the output as determined by S1 and S0. Read back is an image of what the user has sent as output to the module; no checks are performed on the data.
Word 1	Bits 00-15 (00-17)	**Read Back Channel 1** – During normal operation, it is a copy of the output of channel 1. During an EN transition, it is the condition of the output as determined by S1 and S0. Read back is an image of what the user has sent as output to the module; no checks are performed on the data.
Word 2	Bits 00-15 (00-17)	**Read Back Channel 2** – During normal operation, it is a copy of the output of channel 2. During an EN transition, it is the condition of the output as determined by S1 and S0. Read back is an image of what the user has sent as output to the module; no checks are performed on the data.
Word 3	Bits 00-15 (00-17)	**Read Back Channel 3** – During normal operation, it is a copy of the output of channel 3. During an EN transition, it is the condition of the output as determined by S1 and S0. Read back is an image of what the user has sent as output to the module; no checks are performed on the data.
Word 4	Bits 00	Reserved
	Bits 01	**Calibration Done bit (DN). –** This bit is set to 1 after a calibration cycle is completed.
	Bit 02	**Calibration Bad bit (BD). –** This bit is set to 1 if the channel calibration coefficients cannot be saved or read properly.
	Bits 03–07	Set to 0.
	Bits 08–11 (10-12)	Reserved
	Bit 12 (14)	Set to 0
	Bit 13 (15)	**Configuration mode bit (CF)** – This bit is set (1) when the configuration mode is selected (bit 15, word 5 in the block transfer write set to 1). When this bit is set, the module status indicator flashes.
	Bit 14 (16)	**Field Power Off bit (FP)** – This bit is set (1) when the 24V field power fails. When this bit is set (1), the module status indicator flashes.
	Bit 15 (17)	**Power Up (unconfigured state) bit (PU).** – This bit is set (1) when the configuration word is all zeroes (0) due to a reset (adapter power cycle or module insertion) or a cleared configuration word (all 0). When this bit is set, the module status indicator flashes.
Word 5	Bits 00–03	**Wire-Off status bits. (W).** – These bits, when set (1), indicate the corresponding current output channel is open. W0 corresponds to channel 0, W1 corresponds to channel 2, etc.
	Bits 04–07	Set to 0.
	Bits 10–11 (12-13)	**Hold output bits (P).** – These bits are set (1) in response to Q0 or Q1 and a transition of the EN bit. When P0 or P1 is set (1), they indicate that the output is holding at the level in the readback data for the respective channel. These bits return to 0 when the output data matches the readback output data.
	Bits 12–15 (14-17)	Set to 0.

Table 4.11
Analog Output Module (1794-OF4I) Write Configuration Block

Word/Dec. Bit	**15**	**14**	**13**	**12**	**11**	**10**	**09**	**08**	**07**	**06**	**05**	**04**	**03**	**02**	**01**	**00**
Word/Octal Bit	**17**	**16**	**15**	**14**	**13**	**12**	**11**	**10**	**07**	**06**	**05**	**04**	**03**	**02**	**01**	**00**
Write Word 0	EN	S1	S0	0	0	0	0	0	0	0	0	0	0	0	0	0
Word 1	Output Data – Channel 0															
Word 2	Output Data – Channel 1															
Word 3	Output Data – Channel 2															
Word 4	Output Data – Channel 3															
Word 5	Output Chnl 3 Configuration				Output Chnl 2 Configuration				Output Chnl 1 Configuration				Output Chnl 0 Configuration			
Word 6	IC	1	TR	IT	Q3	Q2	Q1	Q0	RV	QK	CK	GO	Channel Number			

Where:
EN = Enable outputs; 0 = output follows S1/S0, 1 = output enabled
IC = Initiate configuration bit
TR = Transparent bit
IT = Interrupt Toggle bit
Q0–3 = Request for outputs to hold
RV = Revert to defaults bit
QK = Quick calibration
CK = Calibration clock
GO = Gain offset select

Table 4.12
Range Selection Bits and Real Time Output Update Rate for the 1794-OF4I Isolated Output Module

Configuration Bits				**Nominal Range**	**Data Type**	**Output Values**		**Update Rate**
MSD		**LSD**				**Hexadecimal**	**Decimal**	
0	0	0	1	4-20mA	2's complement	<0000–7878>	<0000–30840>	5.0ms
0	0	1	0	±10V	2's complement	<8618–79E8>	<–31208–31208>	2.5ms
0	0	1	1	±5V	2's complement	<8618–79E8>	<–31208–31208>	2.5ms
0	1	0	0	0-20mA	2's complement %	0–10000>	0–10000>	5.0ms
0	1	0	1	4-20mA	2's complement %	<0–10000>	<0–10000>	5.0ms
0	1	1	0	0-10V	2's complement %	0–10000>	0–10000>	5.0ms
0	1	1	1	±10V	2's complement	<–10000–10000>	<–10000–10000>	5.0ms
1	0	0	0	0-20mA	binary	0000–F3CF>	0000–62415>	2.5ms
1	0	0	1	4-20mA	binary	0000–F0F1>	0000–61681>	5.0ms
1	0	1	0	0-–10V	binary	0000–F3CF>	0000–62415>	2.5ms
1	0	1	1	0-5V	binary	0000–F3CF>	0000–62415>	2.5ms
1	1	0	0	±20mA	offset binary	<8000–F9E8>	32768–63976>	2.5ms
1	1	0	1	4-20mA	offset binary	<8000–F878>	<32768–63608>	5.0ms

Table 4.12
Range Selection Bits and Real Time Output Update Rate for the 1794-OF4I Isolated Output Module

1	1	1	0	±10V	offset binary	<0618–F9E8>	<1560–63976>	2.5ms
1	1	1	1	±5V	offset binary	<0618–F9E8>	<1560–63976>	2.5ms

Table 4.13
Word/Bit Descriptions for the 1794-OF4I Analog Output Module

Write Word	Decimal Bit (Octal Bit)	Definition
Word 0	Bits 00–14 (00–16)	Not used
	Bits 13–14 (15-16)	**Safe State Source bits (S1/S0).** – When EN is 0, these bits designate the source of the safe state data. Bit 13 = 0, bit 14 = 1 – reset outputs to 0V/0mA (used with 1794-ASB/C) Bit 13 = 1, bit 14 = 1 – hold output at its current level (used with 1794-ASB/C) Bit 13 = 0; bit 14 = 0 – Safe state data is in output data words
	Bit 15 (17)	**Output enable bit (EN).** – When set (1), the outputs are enabled. This bit must be set in order for the real time data to appear at the outputs. If this bit is not set (0), the outputs will be determined by S1/S0.
Word 1	Bits 00–15 (00–17)	**Channel 0 output data.** – The output data is real time data formatted to the selected configuration. (This data is also safe state data when directed by S1 and S0.)
Word 2	Bits 00–15 (00-17)	**Channel 1 output data.** – The output data is real time data formatted to the selected configuration. (This data is also safe state data when directed by S1 and S0.)
Word 3	Bits 00–15 (00-17)	**Channel 2 output data.** – The output data is real time data formatted to the selected configuration. (This data is also safe state data when directed by S1 and S0.)
Word 4	Bits 00–15 (00-17)	**Channel 3 output data.** – The output data is real time data formatted to the selected configuration. (This data is also safe state data when directed by S1 and S0.)
Word 5	Channel Configuration (refer to page 4-66)	
	Bits 00–03	Channel 0 Configuration
	Bits 04–07	Channel 1 Configuration
	Bits 08–11 (10-13)	Channel 2 Configuration
	Bits 12–15 (14-17)	Channel 3 Configuration

Table 4.13
Word/Bit Descriptions for the 1794-OF4I Analog Output Module

Write Word	Decimal Bit (Octal Bit)	Definition
Word 6	Bit 00–03	**Channel calibration selection bit.** When this bit is set (1), the channel can be calibrated using the calibration clock bit (CK). Bit 00 corresponds to output channel 0, bit 01 corresponds to output channel 1, it 02 corresponds to output channel 3, bit 03 corresponds to output channel 4
	Bit 04	**Gain/Offset selection bit (GO).** – When this bit is cleared, a 0 to 1 to 0 transition of the CK bit performs on offset calibration. When this bit is 1, the module is directed to do a gain calibration.
	Bit 05	**Calibration clock bit (CK). –** When this bit is set to 1 (calibration mode), the calibration coeffiicient for the selected channels is accepted. When this bit is reset (0), the accepted calibration coefficients for the selected channels are stored, applied, and the calibration mode exited. Monitor status bits DN and BD for succesful calibration.
	Bit 06	**Quick Calibration bit (QK).** – Normally reset (0). When this bit is set (1) during a calibration sequence, the calibration coefficient is stored to all related configurations for the selected channels. **NOTE:** Although this method of calibration quickly calibrates the selected channels, they will not be within the rated accuracy of the module.
	Bit 07	**Revert to defaults bit (RV).** – Normally reset (0). When set (1) during a calibration procedure, default values for selected channels are used for the calibration coefficient. **NOTE:** They will not be within the rated accuracy of the module.
	Bits 08–11 (10–13)	**Request for hold outputs (Q).** – Channel request bits that instruct an output to hold its output level when EN transitions from 1 to 0 to 1. When EN is 0, outputs go to a safe state dictated by S1/S0. When EN returns to 1, the outputs will hold their level until the output data equals the output level. P0–P3 indicates channels holding. Output read back data shows what level is being held. Q0 = bit 08 (10) = channel 0; Q1 = bit 09 (11) = channel 1, etc.
	Bit 12 (14)	**Interrupt Toggle bit (IT)** – This bit, when set (1), permits interleaving of module interrupts ensuring exchange of critical data when channels are configured for their fastest update times. RTSI and "no low pass filter" must be 0 in order for the module to recognize this feature. This groups data update rates for all channels to the slowest configuration setting of any of the channels. In addition, channel update rates for all channels with a 7.5ms update rate are reduced to 5.0ms. When reset (0), real time sampling and filter features are enabled.
	Bit 13 (15)	**Transparent bit (TR).** – This bit, when set to 1, permits configuration to be changed without using the IC bit.
	Bit 14 (16)	Set to 1
	Bit 15 (17)	**Initiate Configuration bit (IC).** – When set (1), instructs the module to enter configuration mode. Present configuration data prior to or coincident with IC being set. Once IC returns to 0, the configuration is applied and any subquent configuration information is ignored until IC is toggled.

2 Input/2 Output Analog Combo Module (Cat. No. 1794-IF2XOF2I)

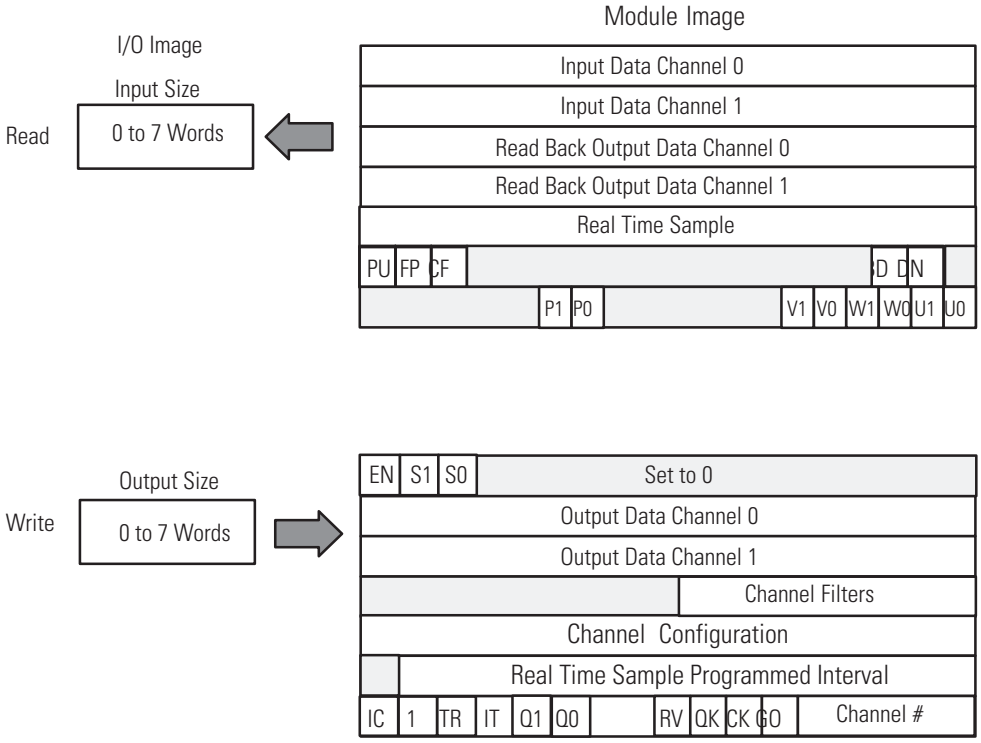


Table 4.14
Analog Combo Module (1794-IF2XOF2I) Read

Word/Dec. Bit	**15**	**14**	**13**	**12**	**11**	**10**	**09**	**08**	**07**	**06**	**05**	**04**	**03**	**02**	**01**	**00**
Word/Octal Bit	**17**	**16**	**15**	**14**	**13**	**12**	**11**	**10**	**07**	**06**	**05**	**04**	**03**	**02**	**01**	**00**
Read Word 0	Input Data Channel 0															
Word 1	Input Data Channel 1															
Word 2	Read Back Output Channel 0															
Word 3	Read Back Output Channel 1															
Word 4	0	Real Time Sample														

Table 4.14
Analog Combo Module (1794-IF2XOF2I) Read

Word 5	PU	FP	CF	0	Reserved				0	0	0	0	0	BD	DN	0
Word 6	0	0	0	0	P1	P0	0	0	0	0	V1	V0	W1	W0	U1	U0

Where:
PU = Power up unconfigured state
FP = Field power off
CF = In configuration mode
BD = Calibration bad
DN = Calibration accepted
P0 and P1 = Output holding in response to Q0 thru Q1
W0 and W1 = Wire off current loop status for input channels 0 and 1 respectively. (Not used on voltage outputs.)
U0 and U1 = Underrange for input channels o and 1 respectively.
V0 and V1 = Overrange for input channels o and 1 respectively.

Table 4.15
Configuring Your Input Channels

Input Channel Configuration										
03	02	01	00	Set these bits for Channel 0						
07	06	05	04	Set these bits for Channel 1						
Bit Settings				**Input Values**	**Data Format**	**% Underrange %Overrange**	**Input Range[(2)]**		**Module Update Rate**	
							Hexadecimal	**Decimal**	**(RTSI = 0)**	**(RTSI = 0) IT = 1**
0	0	0	0	Channel not configured						
0	0	0	1	4–20mA	signed 2's complement	4% Under; 4% Over	<0000–7878>	<0000–30840>	7.5ms	5.0ms
0	0	1	0	±10V	signed 2's complement	2% Under, 2% Over	<831F–7CE1>	<–31969–31969>	2.5ms	2.5ms
0	0	1	1	±5V	signed 2's complement	4% Under, 4% Over	<8618–79E8>	<–31208–31208>	2.5ms	2.5ms
0	1	0	0	0–20mA	signed 2's complement %	0% Under, 4% Over	0–2710>	0–10000>	7.5ms	5.0ms
0	1	0	1	4-20mA	signed 2's complement %	4% Under, 4% Over	<0–2710>	<0–10000>	7.5ms	5.0ms
0	1	1	0	0–10V	signed 2's complement %	0% Under, 2% Over	0–2710>	0–10000>	5.0ms	5.0ms
0	1	1	1	±10V	signed 2's complement %	2% Under, 2% Over	<–D8F0–2710>	<–10000–10000>	5.0ms	5.0ms
1	0	0	0	0–20mA	binary	0% Under, 4% Over	0000–F3CF>	0000–62415>	2.5ms	2.5ms
1	0	0	1	4–20mA[(1)]	binary	4% Under, 4% Over	0000–F0F1>	0000–61681>	7.5ms	5.0ms

Table 4.15
Configuring Your Input Channels

1	0	1	0	0–10V	binary	0% Under, 2% Over	0000–F9C2>	0000–63938>	2.5ms	2.5ms
1	0	1	1	0–5V	binary	0% Under, 4% Over	0000–F3CF>	0000–62415>	2.5ms	2.5ms
1	1	0	0	±20mA	offset binary, 8000H = 0mA	4% Under, 4% Over	<0618–F9E8>	<1560–63976>	2.5ms	2.5ms
1	1	0	1	4–20mA	offset binary, 8000H = 4mA	4% Under, 4% Over	<8000–F878>	<32768–63608>	7.5ms	5.0ms
1	1	1	0	±10V	offset binary, 8000H = 0V	2% Under, 2% Over	<031F–FCE1>	<799–64737>	2.5ms	2.5ms
1	1	1	1	±5V	offset binary, 8000H = 0V	4% Under, 4% Over	<0618–F9E8>	<1560–63976>	2.5ms	2.5ms

(1) Underrange for 4-20mA occurs in the blind area below 0 (3.2mA).

(2) < and > indicate the overrun beyond actual range (about 5%).

Table 4.16
Setting the Input Filter

Bits				**Channel**	
03	02	01	00	Input Channel 0	
07	06	05	04	Input Channel 1	
				A/D Conversion Rate	**Low Pass Filter**
0	0	0	0	1200Hz	No low pass
0	0	0	1	1200Hz	100ms low pass
0	0	1	0	1200Hz	500ms low pass
0	0	1	1	1200Hz	1000ms low pass
0	1	0	0	600Hz	No low pass
0	1	0	1	600Hz	100ms low pass
0	1	1	0	600Hz	500ms low pass
0	1	1	1	600Hz	1000ms low pass
1	0	0	0	300Hz	No low pass
1	0	0	1	300Hz	100ms low pass
1	0	1	0	300Hz	500ms low pass
1	0	1	1	300Hz	1000ms low pass
1	1	0	0	150Hz	No low pass
1	1	0	1	150Hz	100ms low pass
1	1	1	0	150Hz	500ms low pass
1	1	1	1	150Hz	1000ms low pass

Table 4.17
Word/Bit Descriptions for the 1794-IF2XOF2I Isolated Analog Combo Module Read

Write Word	Decimal Bit (Octal Bit)	Definition
Word 0	Bits 00–15 (00–17)	**Input Channel 0 input data** – Real time input data per your configuration
Word 1	Bits 00–15 (00–17)	**Input Channel 1 input data** – Real time input data per your configuration
Word 2	Bits 00–15 (00–17)	**Read Back Output Channel 0** – During normal operation, it is a copy of the output of channel 0. During an EN transition, it is the condition of the output as determined by S1 and S0. **Note:** Read back data is an image of what the user has sent as output to the module; no checks are performed on the data.
Word 3	Bits 00–15 (00–17)	**Read Back Output Channel 1** – During normal operation, it is a copy of the output of channel 1. During an EN transition, it is the condition of the output as determined by S1 and S0. **Note:** Read back data is an image of what the user has sent as output to the module; no checks are performed on the data.
Word 4	Bits 00–15 (00–17)	**Real Time Sample**. The elapsed time in increments programmed by the real time sample interval.
Word 5	Bits 00	Reserved
	Bits 01	**Calibration Done bit (DN). –** This bit is set to 1 after a calibration cycle is completed.
	Bits 02	**Calibration Bad bit (BD). –** This bit is set to 1 if the channel calibration coefficients cannot be saved or read properly.
	Bits 03-07	Set to 0.
	Bits 08-11 (10-12)	Reserved
	Bit 12 (14)	Set to 0
	Bit 13 (15)	**Configuration mode bit (CF)** – This bit is set (1) when the configuration mode is selected (bit 15, word 6 in the block transfer write set to 1). When this bit is set (1), the module status indicator flashes.
	Bit 14 (16)	**Field Power Off bit (FP)** – This bit is set (1) when the 24V field power fails. When this bit is set (1), the module status indicator flashes.
	Bit 15 (17)	**Power Up (unconfigured state) bit (PU).** – This bit is set (1) when the configuration word is all zeroes (0) due to a reset (adapter power cycle or module insertion) or a cleared configuration word (all 0). When this bit is set (1), the module status indicator flashes.

Table 4.17
Word/Bit Descriptions for the 1794-IF2XOF2I Isolated Analog Combo Module Read

Write Word	Decimal Bit (Octal Bit)	Definition
Word 6	Bits 00-01	**Underrange bits (U). –** These bits are set (1) when the input channel is below a preset limit as defined by the configuration selected. U0 (bit 00) corresponds to input channel 0 and U1 (bit 01) corresponds to input channel 1, etc. Refer to Table 4.15.
	Bits 02-03	**Wire-Off status bits. (W). –** These bits, when set (1), indicate the corresponding current output channel is open. W0 (bit 02) corresponds to channel 0, and W1 (bit 03) corresponds to channel 1.
	Bits 04-05	**Overrange bits (V). –** These bits are set (1) when the input channel is above a preset limit as defined by the configuration selected. Bit 04 corresponds to input channel 0 and bit 05 corresponds to input channel 1. Refer to Table 4.15.
	Bits 06-09 (06-11)	Not used. Set to 0.
	Bits 10-11 (12-13)	**Hold output bits (P). –** These bits are set (1) in response to Q0 or Q1 and transition of the EN bit. When P0 or P1 is set (1), they indicate that the output is holding at the level in the readback data for the respective channel. These bits return to 0 when the output data matches the readback output data.
	Bits 12-15 (14-17)	Not used. Set to 0.

Table 4.18
Analog Combo Module (1794-IF2XOF2I) Read

Word/Dec. Bit	**15**	**14**	**13**	**12**	**11**	**10**	**09**	**08**	**07**	**06**	**05**	**04**	**03**	**02**	**01**	**00**
Word/Octal Bit	**17**	**16**	**15**	**14**	**13**	**12**	**11**	**10**	**07**	**06**	**05**	**04**	**03**	**02**	**01**	**00**
Write Word 0	EN	S1	S0	0	0	0	0	0	0	0	0	0	0	0	0	0
Word 1	Output Data Channel 0															
Word 2	Output Data Channel 1															
Word 3	0	0	0	0	0	0	0	0	Input Channel 1 Filter				Input Channel 0 Filter			
Word 4	Output Channel 1 Configuration				Output Channel 0 Configuration				Input Channel 1 Configuration				Input Channel 0 Configuration			
Word 5	0	Real Time Sample Programed Interval														
Word 6	IC	1	TR	IT	Q1	Q2	0	0	RV	QK	CK	GO	Input Channel 0 Configuration			

Where:
EN = Enable outputs; 0 = output follows S1/S0, 1 = output enabled
IC = Initiate configuration bit
IT = Interrupt Toggle bit
TR = Transparent bit
Q0 and Q1 = Request for outputs to hold
RV = Revert to defaults bit
QK = Quick calibration
CK = Calibration clock
GO = Gain offset select

Table 4.19
Configuring Your Outputs for the 1794-IF2XOF2I Analog Combo Module

Configuration Bits				Nominal Range	Data Type	Output Values[1]		Update Rate
MSD		LSD				Hexadecimal	Decimal	
0	0	0	1	4-20mA	2's complement	<0000–7878>	<0000–30840>	5.0ms
0	0	1	0	±10V	2's complement	<8618–79E8>	<–31208–31208>	2.5ms
0	0	1	1	±5V	2's complement	<8618–79E8>	<–31208–31208>	2.5ms
0	1	0	0	0-20mA	2's complement %	0–2710>	0–10000>	5.0ms
0	1	0	1	4-20mA	2's complement %	<0–2710>	<0–10000>	5.0ms
0	1	1	0	0-10V	2's complement %	0–2710>	0–10000>	5.0ms
0	1	1	1	±10V	2's complement %	<–D8F0–2710>	<–10000–10000>	5.0ms
1	0	0	0	0-20mA	binary	0000–F3CF>	0000–62415>	2.5ms
1	0	0	1	4-20mA	binary	0000–F0F1>	0000–61681>	5.0ms
1	0	1	0	0–10V	binary	0000–F3CF>	0000–62415>	2.5ms
1	0	1	1	0-5V	binary	0000–F3CF>	0000–62415>	2.5ms
1	1	0	0	±20mA	offset binary	8000–F9E8>	32768–63976>	2.5ms
1	1	0	1	4-20mA	offset binary	<8000–F878>	<32768–63608>	5.0ms
1	1	1	0	±10V	offset binary	<0618–F9E8>	<1560–63976>	2.5ms
1	1	1	1	±5V	offset binary	<0618–F9E8>	<1560–63976>	2.5ms

(1) < and > indicate the overrun beyond actual range (about 5%).

Table 4.20
Word/Bit Descriptions for the 1794-IF2XOF2I Analog Combo Module Write

Write Word	Decimal Bit (Octal Bit)	Definition
Word 0	Bits 00–14 (00–16)	Not used
	Bit 13–14 (15–16)	**Safe State Source bits (S1/S0). –** When EN is 0, these bits designate the source of the safe state data. Bit 13 = 0, bit 14 = 1 – reset outputs to 0V/0mA (used with 1794-ASB/C) Bit 13 = 1, bit 14 = 1 – hold output at its current level (used with 1794-ASB/C) Bit 13 = 0; bit 14 = 0 – Safe state data is in output data words
	Bit 15 (17)	**Output enable bit (EN). –** When set (1), the outputs are enabled. This bit must be set in order for the real time data to appear at the outputs. If this bit is not set (0), the outputs will be determined by S1/S0.
Word 1	Bits 00–15 (00–17)	**Output Channel 0 data.** Refer to Table 4.19.

Table 4.20
Word/Bit Descriptions for the 1794-IF2XOF2I Analog Combo Module Write

Write Word	Decimal Bit (Octal Bit)	Definition
Word 2	Bits 00–15 (00–17)	**Output Channel 1 data.** Refer to Table 4.19.
Word 3	Input Channels 0 and 1 Filter Selections (refer to Table 4.16)	
	Bits 00–01	Channel 0 Filter Setting
	Bits 04–07	Channel 1 Filter Setting
Word 4	Channel configuration	
	Bits 00–03	**Input Channel 0 Configuration –** Refer to Table 4.15.
	Bits 04–07	**Input Channel 1 Configuration –** Refer to Table 4.15.
	Bits 08–11 (10–13)	**Output Channel 0 Configuration –** Refer to Table 4.19.
	Bits 12–15 (14–17)	**Output Channel 1 Configuration –** Refer to Table 4.19.
Word 5	Bits 00–14 (00–16)	**Real Time Sample Interval –** Programs the interval of the real time sample. Can be varied from 0 to 30 seconds (30000 decimal). Resolution is in ms with granularity in 5ms steps. (see page 4-55)

Table 4.20
Word/Bit Descriptions for the 1794-IF2XOF2I Analog Combo Module Write

Write Word	Decimal Bit (Octal Bit)	Definition
Word 6	Bit 00–03	**Channel calibration selection bit.** When this bit is set (1), the channel can be calibrated using the calibration clock bit (CK). Bit 00 corresponds to input channel 0, bit 01 corresponds to input channel 1, it 02 corresponds to output channel 0, bit 03 corresponds to output channel 1.
	Bit 04	**Gain/Offset selection bit (GO). –** When this bit is cleared, a 0 to 1 to 0 transition of the CK bit performs on offset calibration. When this bit is 1, the module is directed to do a gain calibration.
	Bit 05	**Calibration clock bit (CK). –** When this bit is set to 1 (calibration mode), the calibration coeffiicient for the selected channels is accepted. When this bit is reset (0), the accepted calibration coefficients for the selected channels are stored, applied, and the calibration mode exited. Monitor status bits DN and BD for succesful calibration.
	Bit 06	**Quick Calibration bit (QK). –** Normally reset (0). When this bit is set (1) during a calibration sequence, the calibration coefficient is stored to all related configurations for the selected channels. **NOTE:** This method of calibration quickly calibrates the selected channels, however you will not be within the rated accuracy of the module.
	Bit 07	**Revert to defaults bit (RV). –** Normally reset (0). When set (1) during a calibration procedure, default values for selected channels are used for the calibration coefficient. **NOTE:** You will not be within the rated accuracy of the module.
	Bits 08–09 (10–11)	Not used. Set to 0.
	Bits 10–11 (12–13)	**Request for hold outputs (Q). –** Channel request bits that instruct an output to hold its output level when EN transitions from 1 to 0 to 1. When EN is 0, outputs go to a safe state dictated by S1/S0. When EN returns to 1, the outputs will hold their level until the output data equals the output level. P0–P3 indicates channels holding. Output read back data shows what level is being held. Q0 = bit 08 (10) = channel 0; Q1 = bit 08 (10) = channel 1, etc.
	Bit 12 (14)	**Interrupt Toggle bit (IT) –** This bit, when set (1), permits interleaving of module interrupts ensuring exchange of critical data when channels are configured for their fastest update times. RTSI and “no low pass filter” must be 0 in order for the module to recognize this feature. This groups data update rates for all channels to the slowest configuration setting of any of the channels. In addition, channel update rates for all channels with a 7.5ms update rate are reduced to 5.0ms. When reset (0), real time sampling and filter features are enabled.
	Bit 13 (15)	**Transparent bit (TR). –** This bit, when set to 1, permits configuration to be changed without using the IC bit.
	Bit 15 (17)	**Initiate Configuration bit (IC). –** When set (1), instructs the module to enter configuration mode. Present configuration data prior to or coincident with IC being set. Once IC returns to 0, the configuration is applied and any subquent configuration information is ignored until IC is toggled.

Chapter Summary

In this chapter, you read how to configure your module’s features and enter your data.

Communication and I/O Image Table Mapping with the DeviceNet/ControlNet Adapter

Chapter Objectives

In this chapter, you will read about:

- RSNetWorx and RSLogix software
- I/O structure
- image table mapping
- factory defaults

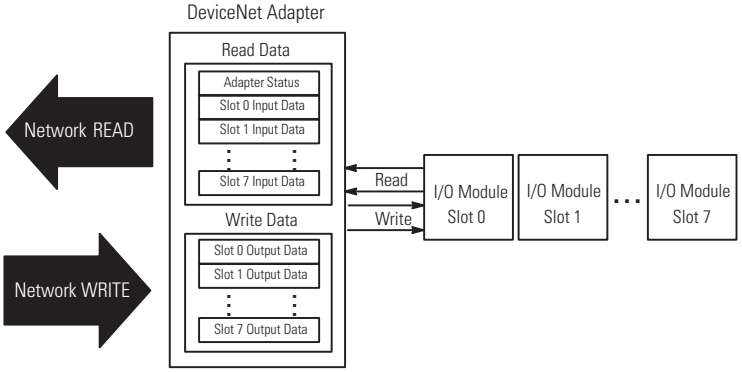
About RSNetWorx and RSLogix

RSNetWorx is a software tool used in conjunction with RSLogix to configure your FLEX I/O DeviceNet or ControlNetadapter and its related modules. This software tool can be connected to the adapter via the DeviceNet network. The Ethernet IP adapter only requires RSLogix to configure the modules.

Polled I/O Structure

Output data is received by the adapter in the order of the installed I/O modules. The Output data for Slot 0 is received first, followed by the Output data for Slot 1, and so on up to slot 7.

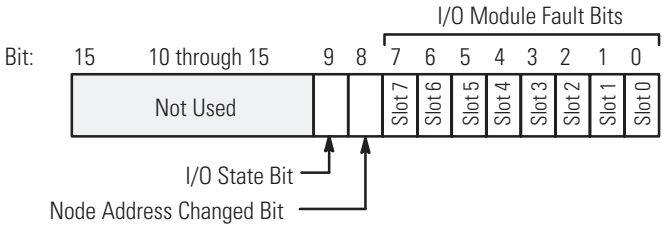
The first word of input data sent by the adapter is the Adapter Status Word. This is followed by the input data from each slot, in the order of installed I/O modules. The Input data from Slot 0 is first after the status word, followed by Input data from Slot 2, and so on to slot 7.



Adapter Input Status Word

The input status word consists of:

- I/O module fault bits – 1 status bit for each slot
- node address changed – 1 bit
- I/O status – 1 bit



The adapter input status word bit descriptions are shown in the following table.

Bit Description	Bit	Explanation
I/O Module Faults	0	This bit is set (1) when an error is detected in slot position 0.
	1	This bit is set (1) when an error is detected in slot position 1.
	2	This bit is set (1) when an error is detected in slot position 2.
	3	This bit is set (1) when an error is detected in slot position 3.
	4	This bit is set (1) when an error is detected in slot position 4.
	5	This bit is set (1) when an error is detected in slot position 5.
	6	This bit is set (1) when an error is detected in slot position 6.
	7	This bit is set (1) when an error is detected in slot position 7.
Node Address Changed	8	This bit is set (1) when the node address switch setting has been changed sing power up.
I/O State	9	Bit = 0 – idle Bit = 1 – run
	10 thru 15	Not used – sent as zeroes.

Possible causes for an **I/O Module Fault** are:

- transmission errors on the FLEX I/O backplane
- a failed module
- a module removed from its terminal base
- incorrect module inserted in a slot position
- the slot is empty

The **node address changed** bit is set when the node address switch setting has been changed since power up. The new node address does not take affect until the adapter has been powered down and then powered back up.

Mapping Data into the Image Table

FLEX I/O analog modules are supported by the DeviceNet adapter.

Module Description	Catalog Number:	For image table mapping refer to:
4 Input Isolated Analog Module	1794-IF4I	page 5-79
4 Output Isolated Analog Module	1794-OF4I	page 5-86
2 in/2 out Isolated Analog Combo Module	1794-IF2XOF2I	page 5-91

4 Input Isolated Analog Module (Cat. No. 1794-IF4I) Image Table Mapping

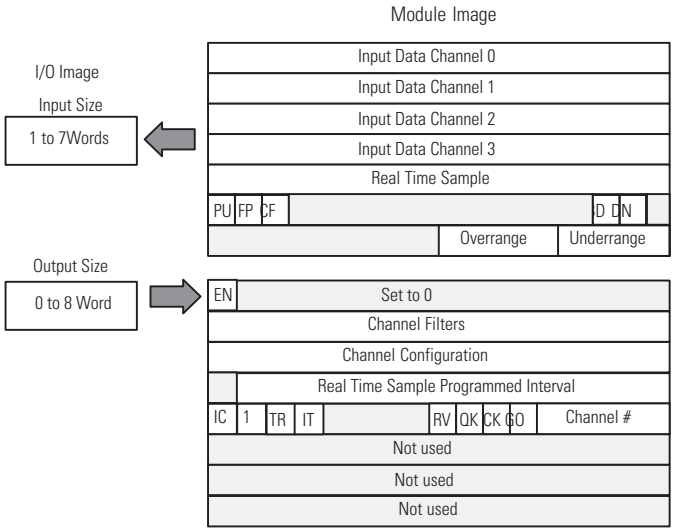


Table 5.1
Analog Input Module (1794-IF4I, 1794-IF4ICFXT) Read

Word/Dec. Bit	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
Word/Octal Bit	**17**	**16**	**15**	**14**	**13**	**12**	**11**	**10**	**07**	**06**	**05**	**04**	**03**	**02**	**01**	**00**
Read Word 1	Analog Value Channel 0															
Word 2	Analog Value Channel 1															
Word 3	Analog Value Channel 2															
Word 4	Analog Value Channel 3															
Word 5	Real Time Sample															
Word 6	PU	FP	CF	0		Reserved			0	0	0	0	0	BD	DN	0
Word 7	0	0	0	0	0	0	0	0	V3	V2	V1	V0	U3	U2	U1	U0

Where:
PU = Power up unconfigured state
FP = Field power off
CF = In configuration mode
BD = Calibration bad
DN = Calibration accepted
U = Under range for specified channel
V = Overrange for specified channel

Table 5.2
Analog Input Module (1794-IF4ICFXT) Write

Dec.	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Oct.	**17**	**16**	**15**	**14**	**13**	**12**	**11**	**10**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Word 0	EN	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Word 1	Channel 3 Filter				Channel 2 Filter				Channel 1 Filter				Channel 0 Filter			
Word 2	Ch 3 Configuration				Ch 2 Configuration				Ch 1 Configuration				Ch 0 Configuration			
Word 3	0	Real Time Sample Interval														
Word 4	IC	1	TR	IT	0	CH	SK	FS	RV	QK	CK	GO	Channel Number			
Word 5	Reserved															

Where :
EN = Enable bit (not used on input module)
IC = Initiate Configuration bit
TR = Transparent bit
IT = Interrupt toggle bit
CH - Chop Mode Disable — use to disable the chop mode. Chop mode used by the module to reduce offset and drift errors. The default is chop mode enabled (0).
SK = FIR Filter Disable — use to disable the FIR filter. The Finite Impulse Response filter is used by the module to improve signal stability. The default is FIR filter enabled (0).
FS = Fast Step Response — use to enable a fast step response algorithm. The fast step response algorithm, upon sensing a step input, uses an averaging method rather than the FIR filter. The FIR goes back into operation once the input has settled. The default is fast step response disabled (0).
RV = Revert to default bit
QK = Quick calibration
CK = Calibration clock
GO = Gain Offset select

Table 5.3
Analog Input Module (1794-IF4I) Write Configuration Block

Word/Dec. Bit	**15**	**14**	**13**	**12**	**11**	**10**	**09**	**08**	**07**	**06**	**05**	**04**	**03**	**02**	**01**	**00**
Word/Octal Bit	**17**	**16**	**15**	**14**	**13**	**12**	**11**	**10**	**07**	**06**	**05**	**04**	**03**	**02**	**01**	**00**
Word 1	EN	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Word 2	Chnl 3 Filter				Chnl 2 Filter				Chnl 1 Filter				Chnl 0 Filter			
Word 3	Chnl 3 Configuration				Chnl 2 Configuration				Chnl 1 Configuration				Chnl 0 Configuration			
Word 4	0	Real Time Sample Programmed Interval														
Word 5	IC	1	TR	IT	0	0	0	0	RV	QK	CK	GO	Channel Number			
Word 6	Not used															
Word 7	Not used															
Word 7	Not used															

Where:
EN = Not used on the 1794-IF4I.
IC = Initiate configuration bit
TR = Transparent bit
IT = Interrupt Toggle bit
RV = Revert to defaults bit
QK = Quick calibration
CK = Calibration clock
GO = Gain offset select

Table 5.4
Setting the Input Filter

Bits				Channel	
03	02	01	00	Input 0	
07	06	05	04	Input 1	
11	10	09	08	Input 2	
15	14	13	12	Input 3	
				A/D Conversion Rate	**Low Pass Filter**
0	0	0	0	1200Hz	No low pass
0	0	0	1	1200Hz	100ms low pass
0	0	1	0	1200Hz	500ms low pass
0	0	1	1	1200Hz	1000ms low pass
0	1	0	0	600Hz	No low pass
0	1	0	1	600Hz	100ms low pass
0	1	1	0	600Hz	500ms low pass
0	1	1	1	600Hz	1000ms low pass
1	0	0	0	300Hz	No low pass
1	0	0	1	300Hz	100ms low pass
1	0	1	0	300Hz	500ms low pass
1	0	1	1	300Hz	1000ms low pass
1	1	0	0	150Hz	No low pass
1	1	0	1	150Hz	100ms low pass
1	1	1	0	150Hz	500ms low pass
1	1	1	1	150Hz	1000ms low pass

Table 5.5
Configuring Your Input Module

Input Channel Configuration									
03	02	01	00	Set these bits for Channel 0					
07	06	05	04	Set these bits for Channel 1					
11	10	09	08	Set these bits for Channel 2					
15	14	13	12	Set these bits for Channel 3					
Bit Settings				**Input Values**	**Data Format**	**% Underrange %Overrange**	**Input Range[(2)]**		**Module Update Rate**	
							Hexadecimal	**Decimal**	**(RTSI = 0)**	**(RTSI = 0) IT = 1**
0	0	0	0	Channel not configured						

Table 5.5
Configuring Your Input Module

0	0	0	1	4–20mA	signed 2's complement	4% Under; 4% Over	<0000–7878>	<0000–30840>	7.5ms	5.0ms
0	0	1	0	±10V	signed 2's complement	2% Under, 2% Over	<831F–7CE1>	<–31969–31969>	2.5ms	2.5ms
0	0	1	1	±5V	signed 2's complement	4% Under, 4% Over	<8618–79E8>	<–31208–31208>	2.5ms	2.5ms
0	1	0	0	0–20mA	signed 2's complement %	0% Under, 4% Over	0–2710>	0–10000>	7.5ms	5.0ms
0	1	0	1	4-20mA	signed 2's complement %	4% Under, 4% Over	<0–2710>	<0–10000>	7.5ms	5.0ms
0	1	1	0	0–10V	signed 2's complement %	0% Under, 2% Over	0–2710>	0–10000>	5.0ms	5.0ms
0	1	1	1	±10V	signed 2's complement %	2% Under, 2% Over	<–D8F0–2710>	<–10000–10000>	5.0ms	5.0ms
1	0	0	0	0–20mA	binary	0% Under, 4% Over	0000–F3CF>	0000–62415>	2.5ms	2.5ms
1	0	0	1	4–20mA[1]	binary	4% Under, 4% Over	0000–F0F1>	0000–61681>	7.5ms	5.0ms
1	0	1	0	0–10V	binary	0% Under, 2% Over	0000–F9C2>	0000–63938>	2.5ms	2.5ms
1	0	1	1	0–5V	binary	0% Under, 4% Over	0000–F3CF>	0000–62415>	2.5ms	2.5ms
1	1	0	0	±20mA	offset binary, 8000H = 0mA	4% Under, 4% Over	<0618–F9E8>	<1560–63976>	2.5ms	2.5ms
1	1	0	1	4–20mA	offset binary, 8000H = 4mA	4% Under, 4% Over	<8000–F878>	<32768–63608>	7.5ms	5.0ms
1	1	1	0	±10V	offset binary, 8000H = 0V	2% Under, 2% Over	<031F–FCE1>	<799–64737>	2.5ms	2.5ms
1	1	1	1	±5V	offset binary, 8000H = 0V	4% Under, 4% Over	<0618–F9E8>	<1560–63976>	2.5ms	2.5ms

(1) Underrange for 4-20mA occurs in the blind area below 0 (3.2mA).

(2) < and > indicate the overrun beyond actual range (about 5%).

Table 5.6
Word/Bit Descriptions for the 1794-IF4I Isolated Analog Input Module

Word	Decimal Bit (Octal Bit)	Definition
Word 1	Bits 00-15 (00-17)	**Channel 0 analog data –** Real time input data per your configuration
Word 2	Bits 00-15 (00-17)	**Channel 1 analog data –** Real time input data per your configuration
Word 3	Bits 00-15 (00-17)	**Channel 2 analog data –** Real time input data per your configuration
Word 4	Bits 00-15 (00-17)	**Channel 3 analog data –** Real time input data per your configuration
Word 5	Bits 00-15 (00-17)	**Real Time Sample**. The elapsed time in increments programmed by the real time sample interval.

Table 5.6
Word/Bit Descriptions for the 1794-IF4I Isolated Analog Input Module

Word	Decimal Bit (Octal Bit)	Definition
Word 6	Bit 00	Reserved
	Bit 01	**Calibration Done bit (DN). –** This bit is set to 1 after a calibration cycle is completed.
	Bit 02	**Calibration Bad bit (BD). –** This bit is set to 1 if the channel calibration coefficients cannot be saved or be read properly.
	Bits 03-07	Set to 0.
	Bits 08-11 (10-12)	Reserved
	Bit 12 (14)	Set to 0.
	Bit 13 (15)	**Configuration mode bit (CF) –** This bit is set (1) when the calibration mode is selected (bit 15, word 5 in the block transfer write set to 1). When this bit is set (1), the module status indicator flashes.
	Bit 14 (16)	**Field Power Off bit (FP) –** This bit is set (1) when the 24V field power fails. When this bit is set (1), the module status indicator flashes.
	Bit 15 (17)	**Power Up (unconfigured state) bit (PU). –** This bit is set (1) when the configuration word is all zeroes (0) due to a reset (adapter power cycle or module insertion) or a cleared configuration word (all 0). When this bit is set (1), the module status indicator flashes.
Word 7	Bits 00-03	**Underrange bits (U). –** These bits are set (1) when the input channel is below a preset limit as defined by the configuration selected. U0 (bit 00) corresponds to input channel 0 and U1 (bit 01) corresponds to input channel 1, etc. Refer to Table 5.5.
	Bits 04-07	**Overrange bits (V). –** These bits are set (1) when the input channel is above a preset limit as defined by the configuration selected. Bit 04 corresponds to input channel 0 and bit 05 corresponds to input channel 1, etc. Refer to Table 5.5.
	Bits 08-15 (10-17)	Not used. Set to 0.
Write Word 1	Bits 00-14 (00-16)	Not used. Set to 0.
	Bit 15 (17)	**Output enable bit (EN). –** Not used in the 1794-IF4I module.
Word 2	**Channels 0 through 3 Filter Selections (refer to Table 5.4)**	
	Bits 00-03	Channel 0 Filter Setting
	Bits 04-07	Channel 1 Filter Setting
	Bits 08-11 (10-13)	Channel 2 Filter Setting
	Bits 12-15 (14-17)	Channel 3 Filter Setting

Table 5.6
Word/Bit Descriptions for the 1794-IF4I Isolated Analog Input Module

Word	Decimal Bit (Octal Bit)	Definition
Word 3	**Channels 0 through 3 Filter Selections (refer to Table 5.5)**	
	Bits 00-03	Channel 0 Configuration
	Bits 04-07	Channel 1 Configuration
	Bits 08-11 (10-13)	Channel 2 Configuration
	Bits 12-15 (14-17)	Channel 3 Configuration
Word 4	Bits 00-14 (00-16)	**Real Time Sample Interval –** Programs the interval of the real time sample. Can be varied from 0 to 30 seconds (30000 decimal). Resolution is in ms with granularity in 5ms steps.
	Bit 15 (17)	Not used. Set to 0.
Word 5	Bit 00-03	**Channel calibration selection bit.** When this bit is set (1), the channel can be calibrated using the calibration clock bit (CK). Bit 00 corresponds to input channel 0, bit 01 corresponds to input channel 1, it 02 corresponds to input channel 2, bit 03 corresponds to input channel 3
	Bit 04	**Gain/Offset selection bit (GO). –** When this bit is cleared, a 0 to 1 to 0 transition of the CK bit performs on offset calibration. When this bit is 1, the module is directed to do a gain calibration.
	Bit 05	**Calibration clock bit (CK). –** When this bit is set to 1 (calibration mode), the calibration coeffiicient for the selected channels is accepted. When this bit is reset (0), the accepted calibration coefficients for the selected channels are stored, applied, and the calibration mode exited. Monitor status bits DN and BD for succesful calibration.
	Bit 06	**Quick Calibration bit (QK). –** Normally reset (0). When this bit is set (1) during a calibration sequence, the calibration coefficient is stored to all related configurations for the selected channels. **NOTE:** This method of calibration quickly calibrates the selected channels, however you will not be within the rated accuracy of the module.
	Bit 07	**Revert to defaults bit (RV). –** Normally reset (0). When set (1) during a calibration procedure, default values for selected channels are used for the calibration coefficient.**NOTE:** You will not be within the rated accuracy of the module.
	Bits 08-11 (10-14)	Not used. Set to 0. For IF4ICFXT only: Bit 8 — **FastStepResponse (FR)** forces the A/D to skip the FIR stage if an input step occurs. An averaging algorithm is temporarily used instead of the FIR filter in the A/D to provide a quicker response. Bit 9 — **FIRFilterDisable (SK)** bypasses the FIR filter stage in the A/D. Bit 10 — **ChopModeDisable (CH)** disables the chop mode in the A/D. Chop mode is used to reduce offsets between input and output of the analog section of the A/D. (1) **Note:** Module level settings that only affect 150 Hz, 300 Hz, and 600 Hz conversion rate settings.

Table 5.6
Word/Bit Descriptions for the 1794-IF4I Isolated Analog Input Module

Word	Decimal Bit (Octal Bit)	Definition
Word 5	Bit 12 (14)	**Interrupt Toggle bit (IT) –** This bit, when set (1), permits interleaving of module interrupts ensuring exchange of critical data when channels are configured for their fastest update times. RTSI and "no low pass filter" must be 0 in order for the module to recognize this feature. This groups data update rates for all channels to the slowest configuration setting of any of the channels. In addition, channel update rates for all channels with a 7.5ms update rate are reduced to 5.0ms. When reset (0), real time sampling and filter features are enabled.
	Bit 13 (15)	**Transparent bit (TR). –** This bit, when set to 1, permits configuration to be changed without using the IC bit.
	Bit 14 (16)	Set to 1.
	Bit 15 (17)	**Initiate Configuration bit (IC). –** When set (1), instructs the module to enter configuration mode. Present configuration data prior to or coincident with IC being set. Once IC returns to 0, the configuration is applied and any subquent configuration information is ignored until IC is toggled.
Words 6, 7 and 8	Bits 00-15 (00-17)	Not used.

(1) For changes in tag values like the CH bit in the IF4ICFXT to take effect, the tag either must be included in a ladder rung or or a configuration download forced using the configuration tab in the RSLogix GUI.

4 Output Isolated Analog Module (Cat. No. 1794-OF4I) Image Table Mapping

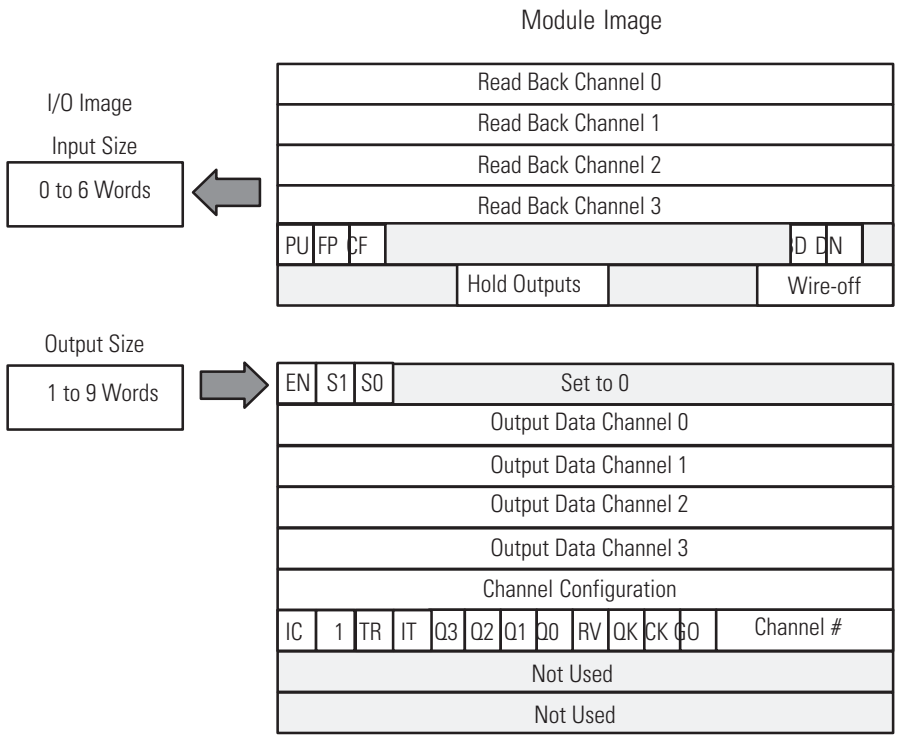


Table 5.7
Analog Output Module (1794-OF4I) Read

Word/Dec. Bit	**15**	**14**	**13**	**12**	**11**	**10**	**09**	**08**	**07**	**06**	**05**	**04**	**03**	**02**	**01**	**00**
Word/Octal Bit	**17**	**16**	**15**	**14**	**13**	**12**	**11**	**10**	**07**	**06**	**05**	**04**	**03**	**02**	**01**	**00**
Read Word 1	Read Back Channel 0															
Word 2	Read Back Channel 1															
Word 3	Read Back Channel 2															
Word 4	Read Back Channel 3															
Word 5	PU	FP	CF	0	Reserved				0	0	0	0	0	BD	DN	0
Word 6	0	0	0	0	P3	P2	P1	P0	0	0	0	0	W3	W2	W1	W0

Where:
PU = Power up unconfigured state
FP = Field power off
CF = In configuration mode
BD = Calibration bad
DN = Calibration accepted
P0 thru P3 = Output holding in response to Q0 thru Q3
W0 thru W3 = Wire off current loop status for channels 0 thru 3 respectively. (Not used on voltage outputs.)

Table 5.8
Analog Output Module (1794-OF4I) Write Configuration Block

Word/Dec. Bit	**15**	**14**	**13**	**12**	**11**	**10**	**09**	**08**	**07**	**06**	**05**	**04**	**03**	**02**	**01**	**00**
Word/Octal Bit	**17**	**16**	**15**	**14**	**13**	**12**	**11**	**10**	**07**	**06**	**05**	**04**	**03**	**02**	**01**	**00**
Write Word 1	EN	S1	S0	0	0	0	0	0	0	0	0	0	0	0	0	0
Word 2	Output Data – Channel 0															
Word 3	Output Data – Channel 1															
Word 4	Output Data – Channel 2															
Word 5	Output Data – Channel 3															
Word 6	Output Chnl 3 Configuration				Output Chnl 2 Configuration				Output Chnl 1 Configuration				Output Chnl 0 Configuration			
Word 7	IC	1	TR	IT	Q3	Q2	Q1	Q0	RV	QK	CK	GO	Channel Number			
Words 8 and 9	Not used															

Where:
EN = Enable outputs; 0 = output follows S1/S0, 1 = output enabled
IC = Initiate configuration bit
TR = Transparent bit
IT = Interrupt Toggle bit
Q0–3 = Request for outputs to hold
RV = Revert to defaults bit
QK = Quick calibration
CK = Calibration clock
GO = Gain offset select

Table 5.9
Configuring Your Outputs for the 1794-OF4I Isolated Output Module

Configuration Bits				**Nominal Range**	**Data Type**	**Output Values**		**Update Rate**
MSD		**LSD**				**Hexadecimal**	**Decimal**	
0	0	0	1	4-20mA	2's complement	<0000–7878>	<0000–30840>	5.0ms
0	0	1	0	±10V	2's complement	<8618–79E8>	<–31208–31208>	2.5ms
0	0	1	1	±5V	2's complement	<8618–79E8>	<–31208–31208>	2.5ms
0	1	0	0	0-20mA	2's complement %	0–10000>	0–10000>	5.0ms
0	1	0	1	4-20mA	2's complement %	<0–10000>	<0–10000>	5.0ms
0	1	1	0	0-10V	2's complement %	0–10000>	0–10000>	5.0ms
0	1	1	1	±10V	2's complement	<–10000–10000>	<–10000–10000>	5.0ms
1	0	0	0	0-20mA	binary	0000–F3CF>	0000–62415>	2.5ms
1	0	0	1	4-20mA	binary	0000–F0F1>	0000–61681>	5.0ms
1	0	1	0	0-–10V	binary	0000–F3CF>	0000–62415>	2.5ms
1	0	1	1	0-5V	binary	0000–F3CF>	0000–62415>	2.5ms
1	1	0	0	±20mA	offset binary	<8000–F9E8>	32768–63976>	2.5ms
1	1	0	1	4-20mA	offset binary	<8000–F878>	<32768–63608>	5.0ms

Table 5.9
Configuring Your Outputs for the 1794-OF4I Isolated Output Module

1	1	1	0	±10V	offset binary	<0618–F9E8>	<1560–63976>	2.5ms
1	1	1	1	±5V	offset binary	<0618–F9E8>	<1560–63976>	2.5ms

Table 5.10
Word/Bit Descriptions for the 1794-OF4I Isolated Analog Output Module

Word	Decimal Bit (Octal Bit)	Definition
Word 1	Bits 00-15 (00-17)	**Read Back Channel 0 –** During normal operation, it is a copy of the output of channel 0. During an EN transition, it is the condition of the output as determined by S1 and S0. Read back is an image of what the user has sent as output to the module; no checks are performed on the data.
Word 2	Bits 00-15 (00-17)	**Read Back Channel 1 –** During normal operation, it is a copy of the output of channel 1. During an EN transition, it is the condition of the output as determined by S1 and S0. Read back is an image of what the user has sent as output to the module; no checks are performed on the data.
Word 3	Bits 00-15 (00-17)	**Read Back Channel 2 –** During normal operation, it is a copy of the output of channel 2. During an EN transition, it is the condition of the output as determined by S1 and S0. Read back is an image of what the user has sent as output to the module; no checks are performed on the data.
Word 4	Bits 00-15 (00-17)	**Read Back Channel 3 –** During normal operation, it is a copy of the output of channel 3. During an EN transition, it is the condition of the output as determined by S1 and S0. Read back is an image of what the user has sent as output to the module; no checks are performed on the data.
Word 5	Bit 00	Reserved
	Bit 01	**Calibration Done bit (DN). –** This bit is set to 1 after a calibration cycle is completed.
	Bit 02	**Calibration Bad bit (BD). –** This bit is set to 1 if the channel calibration coefficients cannot be saved or be read properly.
	Bits 03-07	Set to 0.
	Bits 08-11 (10-12)	Reserved
	Bit 12 (14)	Set to 0.
	Bit 13 (15)	**Configuration mode bit (CF) –** This bit is set (1) when the calibration mode is selected (bit 15, word 5 in the block transfer write set to 1). When this bit is set (1), the module status indicator flashes.
	Bit 14 (16)	**Field Power Off bit (FP) –** This bit is set (1) when the 24V field power fails. When this bit is set (1), the module status indicator flashes.
	Bit 15 (17)	**Power Up (unconfigured state) bit (PU). –** This bit is set (1) when the configuration word is all zeroes (0) due to a reset (adapter power cycle or module insertion) or a cleared configuration word (all 0). When this bit is set (1), the module status indicator flashes.

Table 5.10
Word/Bit Descriptions for the 1794-OF4I Isolated Analog Output Module

Word	Decimal Bit (Octal Bit)	Definition
Word 6	Bits 00-03	**Wire-Off status bits. (W). –** These bits, when set (1), indicate the corresponding current output channel is open. W0 corresponds to channel 0, W1 corresponds to channel 2, etc.
	Bits 04-07	Set to 0.
	Bits 10-11 (12-13)	**Hold output bits (P). –** These bits are set (1) in response to Q0 or Q1 and a transition of the EN bit. When P0 or P1 is set (1), they indicate that the output is holding at the level in the readback data for the respective channel. These bits return to 0 when the output data matches the readback output data.
	Bits 12-15 (14-17)	Set to 0.
Write Word 1	Bits 00-12 (00-14)	Not used.
	Bits 13-14 (15-16)	**Safe State Source bits (S1/S0). –** When EN is 0, these bits designate the source of the safe state data. Bit 13 = 0, bit 14 = 1 – reset outputs to 0V/0mA (used with 1794-ASB/C) Bit 13 = 1, bit 14 = 1 – hold output at its current level (used with 1794-ASB/C Bit 13 = 0; bit 14 = 0 – Safe state data is in output data words
	Bit 15 (17)	**Output enable bit (EN). –** When set (1), the outputs are enabled. This bit must be set in order for the real time data to appear at the outputs. If this bit is not set (0), the outputs will be determined by S1/S0.
Word 2	Bits 00-15 (00-17)	**Channel 0 output data. –** The output data is real time data formatted to the selected configuration. (This data is also safe state data when directed by S! and S0.)
Word 3	Bits 00-15 (00-17)	**Channel 1 output data. –** The output data is real time data formatted to the selected configuration. (This data is also safe state data when directed by S! and S0.)
Word 4	Bits 00-15 (00-17)	**Channel 2 output data. –** The output data is real time data formatted to the selected configuration. (This data is also safe state data when directed by S! and S0.)
Word 5	Bits 00-15 (00-17)	**Channel 3 output data. –** The output data is real time data formatted to the selected configuration. (This data is also safe state data when directed by S! and S0.)
Word 6	**Channel Configuration (refer to Table 5.9)**	
	Bits 00-03	Channel 0 Configuration
	Bits 04-07	Channel 1 Configuration
	Bits 08-11 (10-13)	Channel 2 Configuration
	Bits 12-15 (14-17)	Channel 3 Configuration

Table 5.10
Word/Bit Descriptions for the 1794-OF4I Isolated Analog Output Module

Word	Decimal Bit (Octal Bit)	Definition
Word 7	Bit 00-03	**Channel calibration selection bit.** When this bit is set (1), the channel can be calibrated using the calibration clock bit (CK). Bit 00 corresponds to input channel 0, bit 01 corresponds to input channel 1, it 02 corresponds to input channel 2, bit 03 corresponds to input channel 3
	Bit 04	**Gain/Offset selection bit (GO). –** When this bit is cleared, a 0 to 1 to 0 transition of the CK bit performs on offset calibration. When this bit is 1, the module is directed to do a gain calibration.
	Bit 05	**Calibration clock bit (CK). –** When this bit is set to 1 (calibration mode), the calibration coeffiicient for the selected channels is accepted. When this bit is reset (0), the accepted calibration coefficients for the selected channels are stored, applied, and the calibration mode exited. Monitor status bits DN and BD for succesful calibration.
	Bit 06	**Quick Calibration bit (QK). –** Normally reset (0). When this bit is set (1) during a calibration sequence, the calibration coefficient is stored to all related configurations for the selected channels. **NOTE:** This method of calibration quickly calibrates the selected channels, however you will not be within the rated accuracy of the module.
	Bit 07	**Revert to defaults bit (RV). –** Normally reset (0). When set (1) during a calibration procedure, default values for selected channels are used for the calibration coefficient.**NOTE:** You will not be within the rated accuracy of the module.
	Bits 08-11 (10-14)	**Request for hold outputs (Q). –** Channel request bits that instruct an output to hold its output level when EN transitions from 1 to 0 to 1. When EN is 0, outputs go to a safe state dictated by S1/S0. When EN returns to 1, the outputs will hold their level until the output data equals the output level. P0–P3 indicates channels holding. Output read back data shows what level is being held. Q0 = bit 08 (10) = channel 0; Q1 = bit 08 (10) = channel 1, etc.
Word 7	Bit 12 (14)	**Interrupt Toggle bit (IT) –** This bit, when set (1), permits interleaving of module interrupts ensuring exchange of critical data when channels are configured for their fastest update times. RTSI and "no low pass filter" must be 0 in order for the module to recognize this feature. This groups data update rates for all channels to the slowest configuration setting of any of the channels. In addition, channel update rates for all channels with a 7.5ms update rate are reduced to 5.0ms. When reset (0), real time sampling and filter features are enabled.
	Bit 13 (15)	**Transparent bit (TR). –** This bit, when set to 1, permits configuration to be changed without using the IC bit.
	Bit 14 (16)	Set to 1.
	Bit 15 (17)	**Initiate Configuration bit (IC). –** When set (1), instructs the module to enter configuration mode. Present configuration data prior to or coincident with IC being set. Once IC returns to 0, the configuration is applied and any subquent configuration information is ignored until IC is toggled.
Words 8 and 9	Bits 00-15 (00-17)	Not used.

Isolated Analog Combo Module (Cat. No. 1794-IF2XOF2I Series B) Image Table Mapping

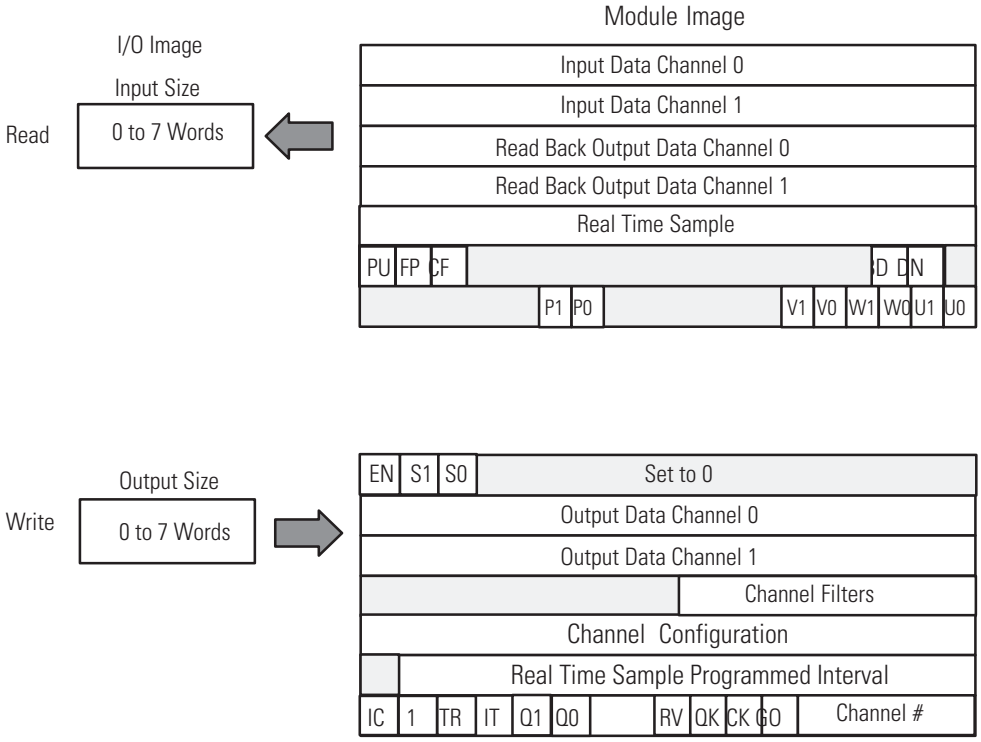


Table 5.11
Analog Combo Module (1794-IF2XOF2I) Read

Word/Dec. Bit	**15**	**14**	**13**	**12**	**11**	**10**	**09**	**08**	**07**	**06**	**05**	**04**	**03**	**02**	**01**	**00**
Word/Octal Bit	**17**	**16**	**15**	**14**	**13**	**12**	**11**	**10**	**07**	**06**	**05**	**04**	**03**	**02**	**01**	**00**
Read Word 0	Input Data Channel 0															
Word 1	Input Data Channel 1															
Word 2	Read Back Output Channel 0															
Word 3	Read Back Output Channel 1															
Word 4	0	Real Time Sample														
Word 5	PU	FP	CF	0	Reserved				0	0	0	0	0	BD	DN	0
Word 6	0	0	0	0	P1	P0	0	0	0	0	V1	V0	W1	W0	U1	U0

Where:
PU = Power up unconfigured state
FP = Field power off
CF = In configuration mode
BD = Calibration bad
DN = Calibration accepted

P0 and P1 = Output holding in response to Q0 thru Q1
W0 and W1 = Wire off current loop status for input channels 0 and 1 respectively. (Not used on voltage outputs.)
U0 and U1 = Underrange for input channels o and 1 respectively.
V0 and V1 = Overrange for input channels o and 1 respectively.

Table 5.12
Configuring Your Input Channels

Input Channel Configuration										
03	02	01	00	Set these bits for Channel 0						
07	06	05	04	Set these bits for Channel 1						
Bit Settings				**Input Values**	**Data Format**	**% Underrange %Overrange**	**Input Range[2]**		**Module Update Rate**	
							Hexadecimal	**Decimal**	**(RTSI = 0)**	**(RTSI = 0) IT = 1**
0	0	0	0	Channel not configured						
0	0	0	1	4–20mA	signed 2's complement	4% Under; 4% Over	<0000–7878>	<0000–30840>	7.5ms	5.0ms
0	0	1	0	±10V	signed 2's complement	2% Under, 2% Over	<831F–7CE1>	<–31969–31969>	2.5ms	2.5ms
0	0	1	1	±5V	signed 2's complement	4% Under, 4% Over	<8618–79E8>	<–31208–31208>	2.5ms	2.5ms
0	1	0	0	0–20mA	signed 2's complement %	0% Under, 4% Over	0–2710>	0–10000>	7.5ms	5.0ms
0	1	0	1	4-20mA	signed 2's complement %	4% Under, 4% Over	<0–2710>	<0–10000>	7.5ms	5.0ms
0	1	1	0	0–10V	signed 2's complement %	0% Under, 2% Over	0–2710>	0–10000>	5.0ms	5.0ms
0	1	1	1	±10V	signed 2's complement %	2% Under, 2% Over	<–D8F0–2710>	<–10000–10000>	5.0ms	5.0ms
1	0	0	0	0–20mA	binary	0% Under, 4% Over	0000–F3CF>	0000–62415>	2.5ms	2.5ms
1	0	0	1	4–20mA[1]	binary	4% Under, 4% Over	0000–F0F1>	0000–61681>	7.5ms	5.0ms
1	0	1	0	0–10V	binary	0% Under, 2% Over	0000–F9C2>	0000–63938>	2.5ms	2.5ms
1	0	1	1	0–5V	binary	0% Under, 4% Over	0000–F3CF>	0000–62415>	2.5ms	2.5ms
1	1	0	0	±20mA	offset binary, 8000H = 0mA	4% Under, 4% Over	<0618–F9E8>	<1560–63976>	2.5ms	2.5ms
1	1	0	1	4–20mA	offset binary, 8000H = 4mA	4% Under, 4% Over	<8000–F878>	<32768–63608>	7.5ms	5.0ms
1	1	1	0	±10V	offset binary, 8000H = 0V	2% Under, 2% Over	<031F–FCE1>	<799–64737>	2.5ms	2.5ms
1	1	1	1	±5V	offset binary, 8000H = 0V	4% Under, 4% Over	<0618–F9E8>	<1560–63976>	2.5ms	2.5ms

(1) Underrange for 4-20mA occurs in the blind area below 0 (3.2mA).

(2) < and > indicate the overrun beyond actual range (about 5%).

Table 5.13
Setting the Input Filter

Bits				**Channel**	
03	02	01	00	Input Channel 0	
07	06	05	04	Input Channel 1	
				A/D Conversion Rate	**Low Pass Filter**
0	0	0	0	1200Hz	No low pass
0	0	0	1	1200Hz	100ms low pass
0	0	1	0	1200Hz	500ms low pass
0	0	1	1	1200Hz	1000ms low pass
0	1	0	0	600Hz	No low pass
0	1	0	1	600Hz	100ms low pass
0	1	1	0	600Hz	500ms low pass

Table 5.13
Setting the Input Filter

0	1	1	1	600Hz	1000ms low pass
1	0	0	0	300Hz	No low pass
1	0	0	1	300Hz	100ms low pass
1	0	1	0	300Hz	500ms low pass
1	0	1	1	300Hz	1000ms low pass
1	1	0	0	150Hz	No low pass
1	1	0	1	150Hz	100ms low pass
1	1	1	0	150Hz	500ms low pass
1	1	1	1	150Hz	1000ms low pass

Table 5.14
Configuring Your Outputs for the 1794-IF2XOF2I Analog Combo Module

Configuration Bits				Nominal Range	Data Type	Output Values(1)		Update Rate
MSD		LSD				Hexadecimal	Decimal	
0	0	0	1	4-20mA	2's complement	<0000–7878>	<0000–30840>	5.0ms
0	0	1	0	±10V	2's complement	<8618–79E8>	<–31208–31208>	2.5ms
0	0	1	1	±5V	2's complement	<8618–79E8>	<–31208–31208>	2.5ms
0	1	0	0	0-20mA	2's complement %	0–10000>	0–10000>	5.0ms
0	1	0	1	4-20mA	2's complement %	<0–10000>	<0–10000>	5.0ms
0	1	1	0	0-10V	2's complement %	0–10000>	0–10000>	5.0ms
0	1	1	1	±10V	2's complement	<–10000-10000>	<–10000–10000>	5.0ms
1	0	0	0	0-20mA	binary	0000–F3CF>	0000–62415>	2.5ms
1	0	0	1	4-20mA	binary	0000–F0F1>	0000–61681>	5.0ms
1	0	1	0	0–10V	binary	0000–F3CF>	0000–62415>	2.5ms
1	0	1	1	0-5V	binary	0000–F3CF>	0000–62415>	2.5ms
1	1	0	0	±20mA	offset binary	8000–F9E8>	32768–63976>	2.5ms
1	1	0	1	4-20mA	offset binary	<8000–F878>	<32768–63608>	5.0ms
1	1	1	0	±10V	offset binary	<0618–F9E8>	<1560–63976>	2.5ms
1	1	1	1	±5V	offset binary	<0618–F9E8>	<1560–63976>	2.5ms

(1) < and > indicate the overrun beyond actual range (about 5%).

Table 5.15
Word/Bit Descriptions for the 1794-IF2XOF2I Isolated Analog Combo Module

Write Word	Decimal Bit (Octal Bit)	Definition
Word 0	Bits 00–15 (00–17)	**Input Channel 0 input data** – 16-bit unipolar; 15-bit plus sign bipolar
Word 1	Bits 00–15 (00–17)	**Input Channel 1 input data –** 16-bit unipolar; 15-bit plus sign bipolar
Word 2	Bits 00–15 (00–17)	**Read Back Output Channel 0 –** During normal operation, it is a copy of the output of channel 0. During an EN transition, it is the condition of the output as determined by S1 and S0.
Word 3	Bits 00–15 (00–17)	**Read Back Output Channel 1 –** During normal operation, it is a copy of the output of channel 1. During an EN transition, it is the condition of the output as determined by S1 and S0.
Word 4	Bits 00–15 (00–17)	**Real Time Sample**. The fixed time period you set telling the module when to provide data to the processor.
Word 5	Bits 00	Reserved
	Bits 01	**Calibration Done bit (DN). –** This bit is set to 1 after a calibration cycle is completed.
	Bits 02	**Calibration Bad bit (BD). –** This bit is set to 1 if the channel calibration coefficients cannot be saved or read properly.
	Bits 03-07	Set to 0.
	Bits 08-11 (10-12)	Reserved
	Bit 12 (14)	Set to 0
	Bit 13 (15)	**Configuration mode bit (CF)** – This bit is set (1) when the configuration mode is selected (bit 15, word 6 in the block transfer write set to 1). When this bit is set (1), the module status indicator flashes.
	Bit 14 (16)	**Field Power Off bit (FP)** – This bit is set (1) when the 24V field power fails. When this bit is set (1), the module status indicator flashes.
	Bit 15 (17)	**Power Up (unconfigured state) bit (PU).** – This bit is set (1) when the configuration word is all zeroes (0) due to a reset (adapter power cycle or module insertion) or a cleared configuration word (all 0). When this bit is set (1), the module status indicator flashes.

Table 5.15
Word/Bit Descriptions for the 1794-IF2XOF2I Isolated Analog Combo Module

Write Word	Decimal Bit (Octal Bit)	Definition
Word 6	Bits 00-01	**Underrange bits (U). –** These bits are set (1) when the input channel is below a preset limit as defined by the configuration selected. U0 (bit 00) corresponds to input channel 0 and U1 (bit 01) corresponds to input channel 1
	Bits 02-03	**Wire-Off status bits. (W). –** These bits, when set (1), indicate the corresponding current output channel is open. W0 (bit 02) corresponds to channel 0, and W1 (bit 03) corresponds to channel 1.
	Bits 04-05	**Overrange bits (V). –** These bits are set (1) when the input channel is above a preset limit as defined by the configuration selected. Bit 04 corresponds to input channel 0 and bit 05 corresponds to input channel 1
	Bits 06-09 (06-11)	Not used. Set to 0.
	Bits 10-11 (12-13)	**Hold output bits (P). –** These bits are set (1) in response to Q0 or Q1 and a transition of the EN bit. When P0 or P1 is set (1), they indicate that the output is holding at the level in the readback data for the respective channel. These bits return to 0 when the output data matches the readback output data.
	Bits 12-15 (14-17)	Not used. Set to 0.
Write Word 1	Bits 00-12 (00-14)	Not used.
	Bits 13-14 (15-16)	**Safe State Source bits (S1/S0). –** When EN is 0, these bits designate the source of the safe state data. Bit 13 = 0, bit 14 = 1 – reset outputs to 0V/0mA Bit 13 = 1, bit 14 = 1 – hold output at its current level
	Bit 15 (17)	**Output enable bit (EN). –** When set (1), the outputs are enabled. This bit must be set in order for the real time data to appear at the outputs. If this bit is not set (0), the outputs will be determined by S1/S0.
Word 2	Bits 00-15 (00-17)	**Output Channel 0 data.** Refer to Table 5.14.
Word 3	Bits 00-15 (00-17)	**Output Channel 1 data.** Refer to Table 5.14.
Word 4	**Input Channels 0 and 1 Filter Selections** Refer to Table 5.13	
	Bits 00-01	Channel 0 Filter Setting
	Bits 04-07	Channel 1 Filter Setting
	Bits 08-15 (11-17)	Set to 0.
Word 5	**Channel Configuration**	
	Bits 00-03	**Input Channel 0 Configuration** Refer to Table 5.12
	Bits 04-07	**Input Channel 1 Configuration** Refer to Table 5.12
	Bits 08-11 (10-13)	**Output Channel 0 Configuration** Refer to Table 5.14.
	Bits 12-15 (14-17)	**Output Channel 1 Configuration** Refer to Table 5.14.

Table 5.15
Word/Bit Descriptions for the 1794-IF2XOF2I Isolated Analog Combo Module

Write Word	Decimal Bit (Octal Bit)	Definition
Word 6	Bits 00-14 (00-16)	**Real Time Sample Interval –** Programs the interval of the real time sample. Can be varied from 0 to 30 seconds (30000 decimal). Resolution is in ms with granularity in 5ms steps.
	Bit 15 (17)	Set to 0.
Word 7	Bits 00-03	**Channel calibration selection bit.** When this bit is set (1), the channel can be calibrated using the initiate calibration bit (IC). Bit 00 corresponds to input channel 0, bit 01 corresponds to input channel 1, it 02 corresponds to output channel 0, bit 03 corresponds to output channel 1
	Bit 04	**Gain/Offset selection bit (GO). –** When this bit is set (1), a reset (0), set (1), reset (0) pattern of the calibration clock bit (CK) causes a **gain** calibration to occur. When this bit is set to 0, a reset (0), set (1), reset (0) pattern of the calibration clock bit (CK) causes an **offset** calibration to occur.
	Bit 05	**Calibration clock bit (CK). –** When this bit is set to 1 (calibration mode), the calibration coeffiicient for the selected channels is accepted. When this bit is reset (0), the accepted calibration coefficients are stored in the selected channels, applied, and the calibration mode exited. Monitor status bits DN and BD for succesful calibration.
	Bit 06	**Quick Calibration bit (QK). –** Normally reset (0). When this bit is set (1) during a calibration sequence, the calibration coefficient is stored to all related configurations for the selected channels. **NOTE:** This method of calibration quickly calibrates the selected channels, you will not be within the rated accuracy of the module.
	Bit 07	**Revert to defaults bit (RV). –** Normally reset (0). When set (1) during a calibration procedure, default values for selected channels are used for the calibration coefficient.
	Bits 08-09 (10-11)	Not used. Set to 0.
	Bits 10-11 (12-13)	**Request for hold outputs (Q). –** Channel request bits that instruct an output to hold its output level when EN transitions from 0 to 1 to 0. When EN is 0, outputs go to a safe state dictated by S1/S0. When EN returns to 1, the outputs will hold their level until the output data equals the output level. P0–P3 indicates channels holding. Output read back data shows what level is being held. Q0 = bit 08 (10) = channel 0; Q1 = bit 08 (10) = channel 1, etc.
	Bit 12 (14)	**Interrupt Toggle bit (IT) –** This bit, when set (1), permits interleaving of module interrupts ensuring exchange of critical data when channels are configured for their fastest update times. RTSI and "no low pass filter" must be 0 in order for the module to recognize this feature. This groups data update rates for all channels to the slowest configuration setting of any of the channels. In addition, channel update rates for all channels with a 7.5ms update rate are reduced to 5.0ms. When reset (0), real time sampling and filter features are enabled.
	Bit 13 (15)	**Transparent bit (TR). –** This bit, when set to 1, permits configuration to be changed without using the IC bit.
	Bit 14 (16)	Set to 1.
	Bit 15 (17)	**Initiate Configuration bit (IC). –** When set (1), instructs the module to enter configuration mode. Present configuration data prior to or coincident with IC being set. Once IC returns to 0, additional configuration information is ignored.
Word 8	Bits 00-15 (00-17)	Not used.

Defaults

Each I/O module has default values associated with it. At default, each module will generate inputs/status and expect outputs/configuration.

Module Defaults for:		Actual Defaults			
Catalog Number	**Description**	**Input Default**	**Output Defaults**	**Input Defaults**	**Output Defaults**
1794-IF4I	4-pt Isolated Analog Input	8	7	4	0
1794-OF4I	4-pt Isolated Analog Output	6	9	4	5
1794-IF2XOF2I	2 in/2 out Isolated Analog Combo	7	8	4	2

Factory defaults are the values available by the adapter.

You can change the I/O data size for a module by reducing the number of words mapped into the adapter module, as shown in real time sizes."

Real time sizes are the settings that provide optimal real time data to the adapter module. These values appear when you:

- first power up the system, and
- no previous stored settings have been applied.

Analog modules have 15 words assigned to them. This is divided into input words/output words. You can reduce the I/O data size to fewer words to increase data transfer over the backplane. For example, a 4 input analog module has 7 words input/8 words output. You can reduce the input words to 4 by not using the real time sample, module status or channel status. Likewise, you can reduce the write words to 0, thus eliminating the conversion rate/filter settings, channel range/data format, real time sample interval and configuration/calibration and unused words.

Input, Output, Status and Configuration Files for Analog Modules when used with ControlNet

Chapter Objectives

In this chapter, you will read about:

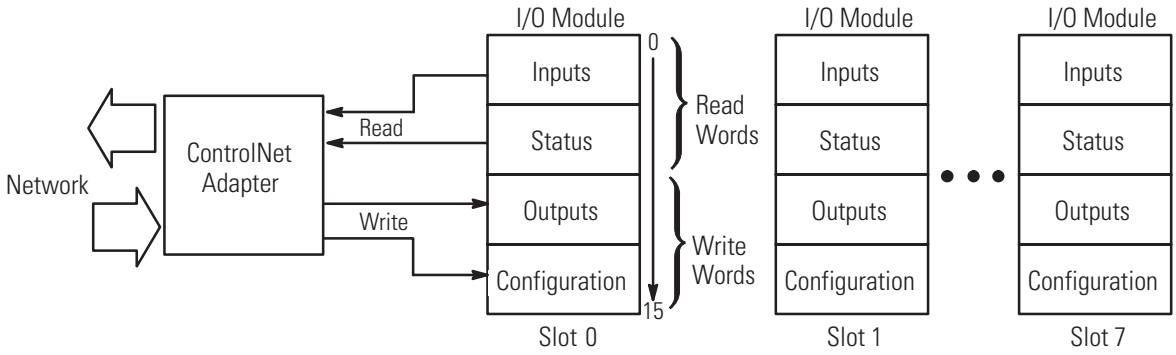
- ControlNet Adapter
- I/O structure
- safe state data
- communication fault data
- idle state behavior
- input data behavior upon module removal

About the ControlNet Adapter

The FLEX I/O ControlNet adapters (cat. no. 1794–ACN15 and –ACNR15) is the interface between up to 8 FLEX I/O modules and a ControlNet processor or scanner. The adapter can support ControlNet real–time data connections to individual modules or module groups. Each connection is independent of the others and can be from different processors or scanners.

Commun ication Over the FLEX I/O Backplane

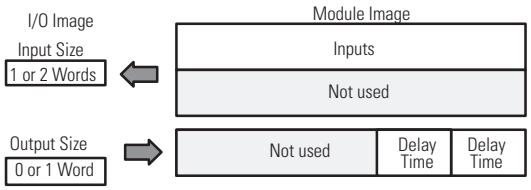
One 1794-ACN15 and -ACNR15 ControlNet adapter can interface with up to eight terminal base units with installed Flex I/O modules, forming a Flex I/O system of up to eight slots. The adapter communicates to other network system components (typically one or more controllers or scanners, and/or programming terminals) over the DeviceNet network. The adapter communicates with its I/O modules over the backplane.



The I/O map for a module is divided into read words and write words. Read words consist of input and status words, and write words consist of output and configuration words. The number of read words or write words can be 0 or more. The length of each I/O module's read words and write words vary in size depending on module complexity. Each I/O module will support at least 1 input word or 1 output word. Status and configuration are optional, depending on the module.

For example, a 16 point discrete input module will have up to 2 read words and 1 write word.

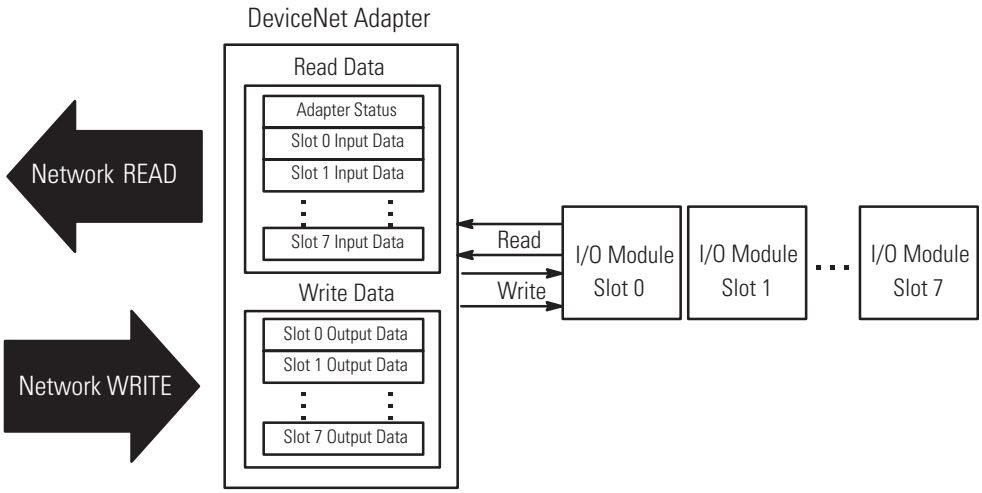
16-point Discrete Input Module



Polled I/O Structure

Output data is received by the adapter in the order of the installed I/O modules. The Output data for Slot 0 is received first, followed by the Output data for Slot 1, and so on up to slot 7.

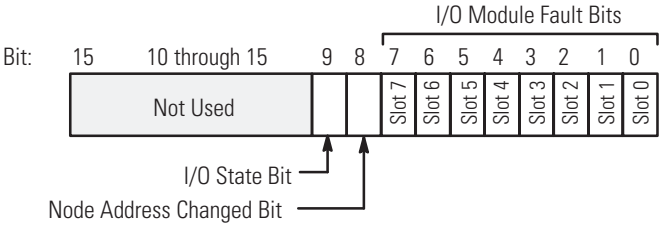
The first word of input data sent by the adapter is the Adapter Status Word. This is followed by the input data from each slot, in the order of the installed I/O modules. The Input data from Slot 0 is first after the status word, followed by Input data from Slot 2, and so on up to slot 7.



Adapter Input Status Word

The input status word consists of:

- I/O module fault bits – 1 status bit for each slot
- node address changed – 1 bit
- I/O status – 1 bit



The adapter input status word bit descriptions are shown in the following table.

Bit Description	Bit	Explanation
I/O Module Fault	0	This bit is set (1) when an error is detected in slot position 0.
	1	This bit is set (1) when an error is detected in slot position 1.
	2	This bit is set (1) when an error is detected in slot position 2.
	3	This bit is set (1) when an error is detected in slot position 3.
	4	This bit is set (1) when an error is detected in slot position 4.
	5	This bit is set (1) when an error is detected in slot position 5.
	6	This bit is set (1) when an error is detected in slot position 6.
	7	This bit is set (1) when an error is detected in slot position 7.
Node Address Changed	8	This bit is set (1) when the node address switch setting has been changed since power up.
I/O State	9	Bit = 0 – idle Bit = 1 – run
	10 – 15	Not used – sent as zeroes.

Possible causes for an **I/O Module Fault** are:

- transmission errors on the FLEX I/O backplane
- a failed module
- a module removed from its terminal base
- incorrect module inserted in a slot position
- the slot is empty

Safe State Data

The ControlNet adapter provides the non-discrete module output data during communication faults or processor idle state. This "safe state data" assures that a known output will be applied to the output devices to maintain a previously designated safe operating condition during the previously mentioned failure modes. The processor or scanner software must include the means to specify this safe state data for each non-discrete module.

Communication Fault Behavior

You can configure the adapter response to a communication fault for each I/O module in its system. Upon detection of a communication fault, the adapter can:

- leave the module output data in its last state (hold last state)
- reset the module output data to zero (reset)
- apply safe state data to the module output

Idle State Behavior

The ControlNet adapter can detect the state of the controlling processor or scanner. Only 2 states can be detected: run mode, or program mode (idle).

When run mode is detected, the adapter copies the output data received from the processor to the corresponding module output. When program mode is detected, the adapter can be configured to:

- leave the module output data in its last state (hold last state)
- reset the module output data to zero (reset)
- apply safe state data to the module output

Input Data Behavior Upon Module Removal

I/O module input data sent by the adapter upon module removal is configurable. The adapter can:

- reset the module output data to zero (reset)
- leave the module output data in the last state before module removal (hold last state)

To find the image table for:	See page:
4 Input Isolated Analog Module (Cat. No. 1794-IF4I)	103
4 Output Isolated Analog Module (1794-OF4I)	108
Isolated Analog Combo Module (1794-IF2XOF2I)	113

4 Input Isolated Analog Module (Cat. No. 1794-IF4I, 1794-IF4IXT, 1794-IF4ICFXT) Table Mapping

Set EN bit Off (0) for Configuration block. Module actions (Reset, Safe State and Hold Last State) are set using programming software.

Table 6.1 Input Map

Dec.	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Oct.	**17**	**16**	**15**	**14**	**13**	**12**	**11**	**10**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Word 0	Analog Value Channel 0															
Word 1	Analog Value Channel 1															
Word 2	Analog Value Channel 2															
Word 3	Analog Value Channel 3															
Word 4	Real Time Sample															
Word 5	PU	FP	CF	0	Reserved				0	0	0	0	0	BD	DN	0
Word 6	0	0	0	0	0	0	0	0	V3	V2	V1	V0	U3	U2	U1	U0

Where :
PU = Power up inconfigured
FP = Field power off
CF = In configuration mode
BD = Bad calibration
DN = Calibration accepted
U = Underrange for specified channel
V = Overrange for specified channel

Table 6.2 Output (Configuration) Map

Dec.	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Oct.	**17**	**16**	**15**	**14**	**13**	**12**	**11**	**10**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Word 0	EN	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Word 1	Channel 3 Filter				Channel 2 Filter				Channel 1 Filter				Channel 0 Filter			
Word 2	Ch 3 Configuration				Ch 2 Configuration				Ch 1 Configuration				Ch 0 Configuration			
Word 3	0	Real Time Sample Interval														
Word 4	IC	1	TR	IT	0	CH	SK	FS	RV	QK	CK	GO	Channel Number			
Word 5	Reserved															

Where :
EN = Enable bit (not used on input module)
IC = Initiate Configuration bit
TR = Transparent bit
IT = Interrupt toggle bit
CH - Chop Mode Disable.
SK = FIR Filter Disable
FS = Fast Step Response
RV = Revert to default bit
QK = Quick calibration
CK = Calibration clock
GO = Gain Offset select

Table 6.3
Word/Bit Descriptions for Isolated Analog Input Module

Word	**Decimal Bit (Octal Bit)**	**Definition**
Input Word 0	Bits 00-15 (00-17)	**Channel 0 analog data –** Real time input data per your configuration
Word 1	Bits 00-15 (00-17)	**Channel 1 analog data –** Real time input data per your configuration
Word 2	Bits 00-15 (00-17)	**Channel 2 analog data –** Real time input data per your configuration
Word 3	Bits 00-15 (00-17)	**Channel 3 analog data –** Real time input data per your configuration
Word 4	Bits 00-15 (00-17)	**Real Time Sample**. The elapsed time in increments programmed by the real time sample interval.

Table 6.3
Word/Bit Descriptions for Isolated Analog Input Module

Word	Decimal Bit (Octal Bit)	Definition
Word 5	Bit 00	Reserved
	Bit 01	**Calibration Done bit (DN). –** This bit is set to 1 after a calibration cycle is completed.
	Bit 02	**Calibration Bad bit (BD). –** This bit is set to 1 if the channel calibration coefficients cannot be saved or be read properly.
	Bits 03-07	Set to 0.
	Bits 08-11 (10-12)	Reserved
	Bit 12 (14)	Set to 0.
	Bit 13 (15)	**Configuration mode bit (CF) –** This bit is set (1) when the calibration mode is selected (bit 15, word 5 in the block transfer write set to 1). When this bit is set (1), the module status indicator flashes.
	Bit 14 (16)	**Field Power Off bit (FP) –** This bit is set (1) when the 24V field power fails. When this bit is set (1), the module status indicator flashes.
	Bit 15 (17)	**Power Up (unconfigured state) bit (PU). –** This bit is set (1) when the configuration word is all zeroes (0) due to a reset (adapter power cycle or module insertion) or a cleared configuration word (all 0). When this bit is set (1), the module status indicator flashes.
Word 6	Bits 00-03	**Underrange bits (U). –** These bits are set (1) when the input channel is below a preset limit as defined by the configuration selected. U0 (bit 00) corresponds to input channel 0 and U1 (bit 01) corresponds to input channel 1, etc.
	Bits 04-07	**Overrange bits (V). –** These bits are set (1) when the input channel is above a preset limit as defined by the configuration selected. Bit 04 corresponds to input channel 0 and bit 05 corresponds to input channel 1, etc.
	Bits 08-15 (10-17)	Not used. Set to 0.

Configuration Word 0	Bits 00-14 (00-16)	Not used. Set to 0.
	Bit 15 (17)	**Output enable bit (EN). –** Not used in the 1794-IF4I module.
Word 1	**Channels 0 through 3 Filter Selections**	
	Bits 00-03	Channel 0 Filter Setting
	Bits 04-07	Channel 1 Filter Setting
	Bits 08-11 (10-13)	Channel 2 Filter Setting
	Bits 12-15 (14-17)	Channel 3 Filter Setting

Table 6.3
Word/Bit Descriptions for Isolated Analog Input Module

Word	Decimal Bit (Octal Bit)	Definition
Word 2	**Channel Configuration**	
	Bits 00-03	Channel 0 Configuration
	Bits 04-07	Channel 1 Configuration
	Bits 08-11 (10-13)	Channel 2 Configuration
	Bits 12-15 (14-17)	Channel 3 Configuration
Word 3	Bits 00-14 (00-16)	**Real Time Sample Interval** – Programs the interval of the real time sample. Can be varied from 0 to 30 seconds (30000 decimal). Resolution is in ms with granularity in 5ms steps.
	Bit 15 (17)	Not used. Set to 0.

Table 6.3
Word/Bit Descriptions for Isolated Analog Input Module

Word	Decimal Bit (Octal Bit)	Definition
Word 4	Bit 00-03	**Channel calibration selection bit.** When this bit is set (1), the channel can be calibrated using the calibration clock bit (CK). Bit 00 corresponds to input channel 0, bit 01 corresponds to input channel 1, it 02 corresponds to input channel 2, bit 03 corresponds to input channel 3
	Bit 04	**Gain/Offset selection bit (GO). –** When this bit is cleared, a 0 to 1 to 0 transition of the CK bit performs on offset calibration. When this bit is 1, the module is directed to do a gain calibration.
	Bit 05	**Calibration clock bit (CK). –** When this bit is set to 1 (calibration mode), the calibration coeffiicient for the selected channels is accepted. When this bit is reset (0), the accepted calibration coefficients for the selected channels are stored, applied, and the calibration mode exited. Monitor status bits DN and BD for succesful calibration.
	Bit 06	**Quick Calibration bit (QK). –** Normally reset (0). When this bit is set (1) during a calibration sequence, the calibration coefficient is stored to all related configurations for the selected channels. **NOTE:** This method of calibration quickly calibrates the selected channels, however you will not be within the rated accuracy of the module.
	Bit 07	**Revert to defaults bit (RV). –** Normally reset (0). When set (1) during a calibration procedure, default values for selected channels are used for the calibration coefficient.**NOTE:** You will not be within the rated accuracy of the module.
	Bit 08	1794-IF4I - Not used. Set to 0. 1794-IF4ICFXT - **Fast Step Response (FS).** - Use to enable a fast step response algorithm. The fast step response algorithm, upon sensing a step input, uses an averaging method rather than the FIR filter. The FIR goes back into operation once the input has settled. The default is fast step response disabled (0).
	Bit 09	1794-IF4I - Not used. Set to 0. 1794-IF4ICFXT - **FIR Filter Disable (SK).** - Use to disable the FIR filter. The Finite Impulse Response filter is used by the module to improve signal stability. The default is FIR filter enabled (0).
	Bit 10	1794-IF4I - Not used. Set to 0. 1794-IF4ICFXT - **Chop Mode Disable (CH).** -Use to disable the chop mode. Chop mode used by the module to reduce offset and drift errors. The default is chop mode enabled (0).
	Bit 11	Not used. Set to 0.
	Bit 12 (14)	**Interrupt Toggle bit (IT) –** This bit, when set (1), permits interleaving of module interrupts ensuring exchange of critical data when channels are configured for their fastest update times. RTSI and “no low pass filter” must be 0 in order for the module to recognize this feature. This groups data update rates for all channels to the slowest configuration setting of any of the channels. In addition, channel update rates for all channels with a 7.5ms update rate are reduced to 5.0ms. When reset (0), real time sampling and filter features are enabled.
	Bit 13 (15)	**Transparent bit (TR). –** This bit, when set to 1, permits configuration to be changed without using the IC bit.
	Bit 14 (16)	Set to 1.
	Bit 15 (17)	**Initiate Configuration bit (IC). –** When set (1), instructs the module to enter configuration mode. Present configuration data prior to or coincident with IC being set. Once IC returns to 0, the configuration is applied and any subquent configuration information is ignored until IC is toggled.

Table 6.3
Word/Bit Descriptions for Isolated Analog Input Module

Word	Decimal Bit (Octal Bit)	Definition

Table 6.4
Setting the Input Filter

Bits				Channel	
03	02	01	00	Input 0	
07	06	05	04	Input 1	
11	10	09	08	Input 2	
15	14	13	12	Input 3	
				A/D Conversion Rate	**Low Pass Filter**
0	0	0	0	1200Hz	No low pass
0	0	0	1	1200Hz	100ms low pass
0	0	1	0	1200Hz	500ms low pass
0	0	1	1	1200Hz	1000ms low pass
0	1	0	0	600Hz	No low pass
0	1	0	1	600Hz	100ms low pass
0	1	1	0	600Hz	500ms low pass
0	1	1	1	600Hz	1000ms low pass
1	0	0	0	300Hz	No low pass
1	0	0	1	300Hz	100ms low pass
1	0	1	0	300Hz	500ms low pass
1	0	1	1	300Hz	1000ms low pass
1	1	0	0	150Hz	No low pass
1	1	0	1	150Hz	100ms low pass
1	1	1	0	150Hz	500ms low pass
1	1	1	1	150Hz	1000ms low pass

Table 6.5
Configuring Your Input Module

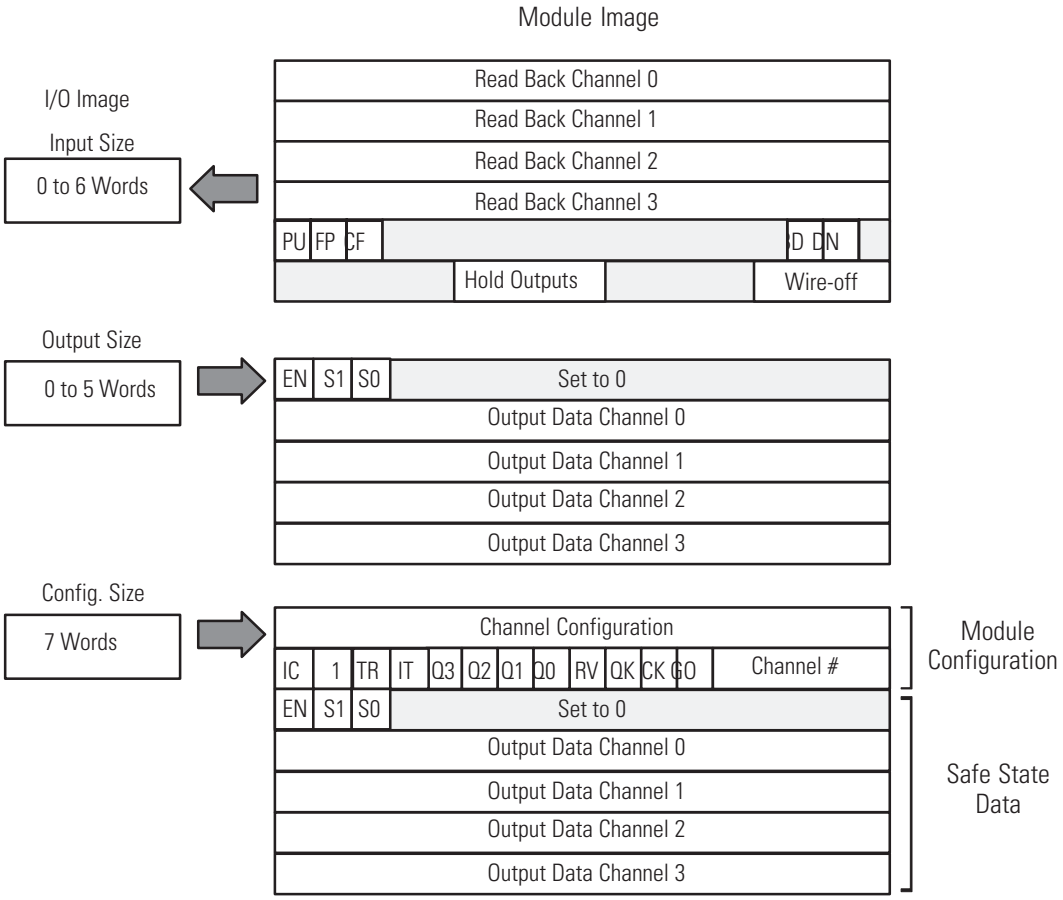
Input Channel Configuration				
03	02	01	00	Set these bits for Channel 0
07	06	05	04	Set these bits for Channel 1
11	10	09	08	Set these bits for Channel 2
15	14	13	12	Set these bits for Channel 3

Table 6.5
Configuring Your Input Module

Bit Settings				**Input Values**	**Data Format**	**% Underrange %Overrange**	**Input Range**		**Module Update Rate**
							Hexadecimal	**Decimal**	**(RTS = 0)**
0	0	0	0	Channel not configured					
0	0	0	1	4–20mA	signed 2's complement	4% Under; 4% Over	<0000–7878>	<0000–30840>	7.5ms
0	0	1	0	±10V	signed 2's complement	2% Under, 2% Over	<831F–7CE1>	<–31969–31969>	2.5ms
0	0	1	1	±5V	signed 2's complement	4% Under, 4% Over	<8618–79E8>	<–31208–31208>	2.5ms
0	1	0	0	0–20mA	signed 2's complement %	0% Under, 4% Over	0–10000>	0–10000>	7.5ms
0	1	0	1	4-20mA	signed 2's complement %	4% Under, 4% Over	<0–10000>	<0–10000>	7.5ms
0	1	1	0	0–10V	signed 2's complement %	0% Under, 2% Over	0–10000>	0–10000>	5.0ms
0	1	1	1	±10V	signed 2's complement %	2% Under, 2% Over	<–10000–10000>	<–10000–10000>	5.0ms
1	0	0	0	0–20mA	binary	0% Under, 4% Over	0000–F3CF>	0000–62415>	2.5ms
1	0	0	1	4–20mA[1]	binary	4% Under, 4% Over	0000–F0F1>	0000–61681>	7.5ms
1	0	1	0	0–10V	binary	0% Under, 2% Over	0000–F9C2>	0000–62415>	2.5ms
1	0	1	1	0–5V	binary	0% Under, 4% Over	0000–F3CF>	0000–62415>	2.5ms
1	1	0	0	±20mA	offset binary, 8000H = 0mA	4% Under, 4% Over	<0618–F9E8>	32768–63976>	2.5ms
1	1	0	1	4–20mA	offset binary, 8000H = 4mA	4% Under, 4% Over	<8000–F878>	<32768–63608>	7.5ms
1	1	1	0	±10V	offset binary, 8000H = 0V	2% Under, 2% Over	<031F–FCE1>	<799–64737>	2.5ms
1	1	1	1	±5V	offset binary, 8000H = 0V	4% Under, 4% Over	<0618–F9E8>	<1560–63976>	2.5ms

(1) Underrange for 4-20mA occurs in the blind area below 0 (3.2mA).

4 Output Isolated Analog Module (Cat. No. 1794-OF4I) Image Table Mapping



Set EN bit Off (0) for Configuration block
Set EN bit On (1) for Output block
S0 and S1 bits are not used in ControlNet applications. Set to Off (0).
Module actions (Reset, Safe State and Hold Last State) are set using programming software.

Table 6.6
Word/Bit Descriptions for the 1794-OF4I Isolated Analog Output Module

Word	Decimal Bit (Octal Bit)	Definition
Input Word 0	Bits 00-15 (00-17)	**Read Back Channel 0 –** During normal operation, it is a copy of the output of channel 0. During an EN transition, it is the condition of the output as determined by S1 and S0. Read back is an image of what the user has sent as output to the module; no checks are performed on the data.
Word 1	Bits 00-15 (00-17)	**Read Back Channel 1 –** During normal operation, it is a copy of the output of channel 1. During an EN transition, it is the condition of the output as determined by S1 and S0. Read back is an image of what the user has sent as output to the module; no checks are performed on the data.
Word 2	Bits 00-15 (00-17)	**Read Back Channel 2 –** During normal operation, it is a copy of the output of channel 2. During an EN transition, it is the condition of the output as determined by S1 and S0. Read back is an image of what the user has sent as output to the module; no checks are performed on the data.
Word 3	Bits 00-15 (00-17)	**Read Back Channel 3 –** During normal operation, it is a copy of the output of channel 3. During an EN transition, it is the condition of the output as determined by S1 and S0. Read back is an image of what the user has sent as output to the module; no checks are performed on the data.
Word 4	Bit 00	Reserved
	Bit 01	**Calibration Done bit (DN). –** This bit is set to 1 after a calibration cycle is completed.
	Bit 02	**Calibration Bad bit (BD). –** This bit is set to 1 if the channel calibration coefficients cannot be saved or be read properly.
	Bits 03-07	Set to 0.
	Bits 08-11 (10-12)	Reserved
	Bit 12 (14)	Set to 0.
	Bit 13 (15)	**Configuration mode bit (CF) –** This bit is set (1) when the calibration mode is selected (bit 15, word 5 in the block transfer write set to 1). When this bit is set (1), the module status indicator flashes.
	Bit 14 (16)	**Field Power Off bit (FP) –** This bit is set (1) when the 24V field power fails. When this bit is set (1), the module status indicator flashes.
	Bit 15 (17)	**Power Up (unconfigured state) bit (PU). –** This bit is set (1) when the configuration word is all zeroes (0) due to a reset (adapter power cycle or module insertion) or a cleared configuration word (all 0). When this bit is set (1), the module status indicator flashes.

Table 6.6
Word/Bit Descriptions for the 1794-OF4I Isolated Analog Output Module

Word	Decimal Bit (Octal Bit)	Definition
Word 5	Bits 00-03	**Wire-Off status bits. (W). –** These bits, when set (1), indicate the corresponding current output channel is open. W0 corresponds to channel 0, W1 corresponds to channel 2, etc.
	Bits 04-07	Set to 0.
	Bits 10-11 (12-13)	**Hold output bits (P). –** These bits are set (1) in response to Q0 or Q1 and a transition of the EN bit. When P0 or P1 is set (1), they indicate that the output is holding at the level in the readback data for the respective channel. These bits return to 0 when the output data matches the readback output data.
	Bits 12-15 (14-17)	Set to 0.
Output Word 0	Bits 00-12 (00-14)	Not used.
	Bits 13-14 (15-16)	**Safe State Source bits (S1/S0). –** Not used in ControlNet applications. Turn these bits off (i.e. set to 0)
	Bit 15 (17)	**Output enable bit (EN)** Set this bit off (0) for the configuration block. Set this bit on (1) for the output block.
Word 1	Bits 00-15 (00-17)	**Channel 0 output data. –** The output data is real time data formatted to the selected configuration. (This data is also safe state data when directed by S! and S0.)
Word 2	Bits 00-15 (00-17)	**Channel 1 output data. –** The output data is real time data formatted to the selected configuration. (This data is also safe state data when directed by S1 and S0.)
Word 3	Bits 00-15 (00-17)	**Channel 2 output data. –** The output data is real time data formatted to the selected configuration. (This data is also safe state data when directed by S1 and S0.)
Word 4	Bits 00-15 (00-17)	**Channel 3 output data. –** The output data is real time data formatted to the selected configuration. (This data is also safe state data when directed by S1 and S0.)
Configuration Word 0	**Channel Configuration (refer to Table 6.5)**	
	Bits 00-03	Channel 0 Configuration
	Bits 04-07	Channel 1 Configuration
	Bits 08-11 (10-13)	Channel 2 Configuration
	Bits 12-15 (14-17)	Channel 3 Configuration

Table 6.6
Word/Bit Descriptions for the 1794-OF4I Isolated Analog Output Module

Word	Decimal Bit (Octal Bit)	Definition
Word 1	Bit 00-03	**Channel calibration selection bit.** When this bit is set (1), the channel can be calibrated using the calibration clock bit (CK). Bit 00 corresponds to input channel 0, bit 01 corresponds to input channel 1, bit 02 corresponds to input channel 3, bit 03 corresponds to input channel 4
	Bit 04	**Gain/Offset selection bit (GO). –** When this bit is cleared, a 0 to 1 to 0 transition of the CK bit performs on offset calibration. When this bit is 1, the module is directed to do a gain calibration.
	Bit 05	**Calibration clock bit (CK). –** When this bit is set to 1 (calibration mode), the calibration coeffiicient for the selected channels is accepted. When this bit is reset (0), the accepted calibration coefficients for the selected channels are stored, applied, and the calibration mode exited. Monitor status bits DN and BD for succesful calibration.
	Bit 06	**Quick Calibration bit (QK). –** Normally reset (0). When this bit is set (1) during a calibration sequence, the calibration coefficient is stored to all related configurations for the selected channels. **NOTE:** This method of calibration quickly calibrates the selected channels, however you will not be within the rated accuracy of the module.
	Bit 07	**Revert to defaults bit (RV). –** Normally reset (0). When set (1) during a calibration procedure, default values for selected channels are used for the calibration coefficient.**NOTE:** You will not be within the rated accuracy of the module.
	Bits 08-11 (10-14)	**Request for hold outputs (Q). –** Channel request bits that instruct an output to hold its output level when EN transitions from 1 to 0 to 1. When EN is 0, outputs go to a safe state dictated by S1/S0. When EN returns to 1, the outputs will hold their level until the output data equals the output level. P0–P3 indicates channels holding. Output read back data shows what level is being held. Q0 = bit 08 (10) = channel 0; Q1 = bit 08 (10) = channel 1, etc.
	Bit 12 (14)	**Interrupt Toggle bit (IT) –** This bit, when set (1), permits interleaving of module interrupts ensuring exchange of critical data when channels are configured for their fastest update times. RTSI and "no low pass filter" must be 0 in order for the module to recognize this feature. This groups data update rates for all channels to the slowest configuration setting of any of the channels. In addition, channel update rates for all channels with a 7.5ms update rate are reduced to 5.0ms. When reset (0), real time sampling and filter features are enabled.
	Bit 13 (15)	**Transparent bit (TR). –** This bit, when set to 1, permits configuration to be changed without using the IC bit.
	Bit 14 (16)	Set to 1.
	Bit 15 (17)	**Initiate Configuration bit (IC). –** When set (1), instructs the module to enter configuration mode. Present configuration data prior to or coincident with IC being set. Once IC returns to 0, the configuration is applied and any subquent configuration information is ignored until IC is toggled.

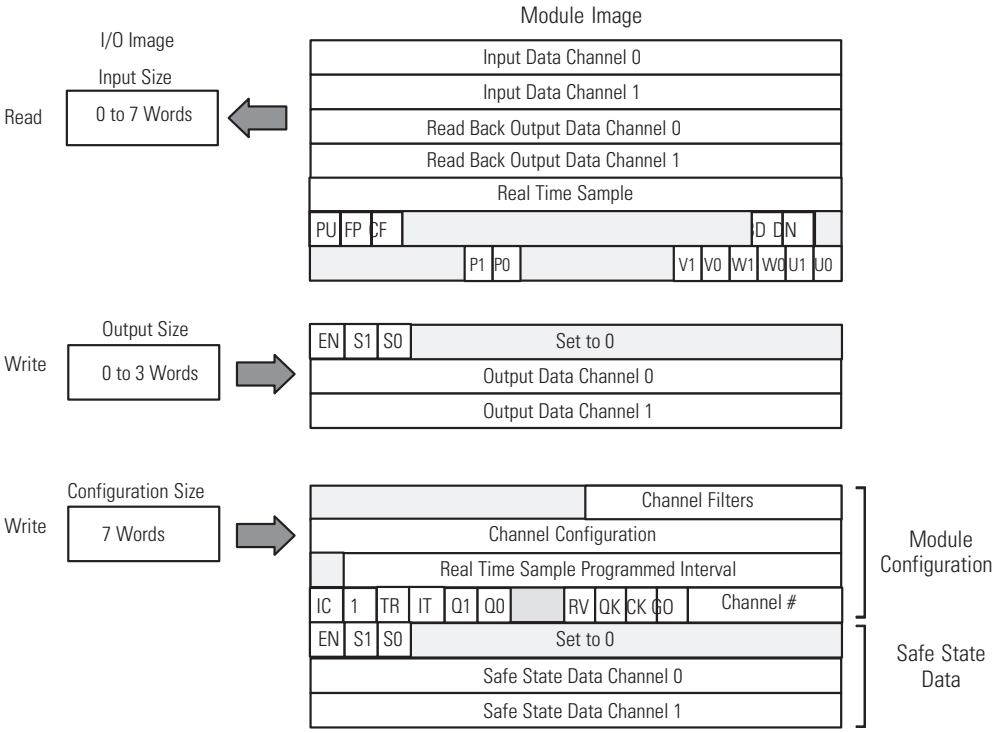
Table 6.6
Word/Bit Descriptions for the 1794-OF4I Isolated Analog Output Module

Word	Decimal Bit (Octal Bit)	Definition
Word 2	Bits 00-14 (00-16)	Not used
	Bits 13-14 (15-16)	**Safe State Source bits (S1/S0)** - Not used in ControlNet applications. Turn these bits off (i.e. set to 0)
	Bit 15 (17)	**Output Enable bit (EN)** Set this bit off (0) for the output block Set this bit on (1) for the configuration block
Word 3	Bits 00-15 (00-17)	**Channel 0 output data. –** The output data is real time data formatted to the selected configuration. (This data is also safe state data when directed by S1 and S0.)
Word 4	Bits 00-15 (00-17)	**Channel 1 output data. –** The output data is real time data formatted to the selected configuration. (This data is also safe state data when directed by S1 and S0.)
Word 5	Bits 00-15 (00-17)	**Channel 2 output data. –** The output data is real time data formatted to the selected configuration. (This data is also safe state data when directed by S1 and S0.)
Word 6	Bits 00-15 (00-17)	**Channel 3 output data. –** The output data is real time data formatted to the selected configuration. (This data is also safe state data when directed by S1 and S0.)

Table 6.7
Configuring Your Outputs for the 1794-OF4I Isolated Output Module

Configuration Bits				Nominal Range	Data Type	Output Values		Update Rate
MSD		LSD				Hexadecimal	Decimal	
0	0	0	1	4-20mA	2's complement	<0000–7878>	<0000–30840>	5.0ms
0	0	1	0	±10V	2's complement	<8618–79E8>	<–31208–31208>	2.5ms
0	0	1	1	±5V	2's complement	<8618–79E8>	<–31208–31208>	2.5ms
0	1	0	0	0-20mA	2's complement %	0–10000>	0–10000>	5.0ms
0	1	0	1	4-20mA	2's complement %	<0–10000>	<0–10000>	5.0ms
0	1	1	0	0-10V	2's complement %	0–10000>	0–10000>	5.0ms
0	1	1	1	±10V	2's complement	<–10000–10000>	<–10000–10000>	5.0ms
1	0	0	0	0-20mA	binary	0000–F3CF>	0000–62415>	2.5ms
1	0	0	1	4-20mA	binary	0000–F0F1>	0000–61681>	5.0ms
1	0	1	0	0-–10V	binary	0000–F3CF>	0000–62415>	2.5ms
1	0	1	1	0-5V	binary	0000–F3CF>	0000–62415>	2.5ms
1	1	0	0	±20mA	offset binary	<8000–F9E8>	32768–63976>	2.5ms
1	1	0	1	4-20mA	offset binary	<8000–F878>	<32768–63608>	5.0ms
1	1	1	0	±10V	offset binary	<0618–F9E8>	<1560–63976>	2.5ms
1	1	1	1	±5V	offset binary	<0618–F9E8>	<1560–63976>	2.5ms

Isolated Analog Combo Module (Cat. No. 1794-IF2XOF2I) Image Table Mapping



Set EN bit Off (0) for Configuration block
Set EN bit On (1) for Output block
S0 and S1 bits are not used in ControlNet applications. Set to Off (0).
Module actions (Reset, Safe State and Hold Last State) are set using programming software.

Table 6.8
Word/Bit Descriptions for the 1794-IF2XOF2I Isolated Analog Combo Module

Write Word	Decimal Bit (Octal Bit)	Definition
Input Word 0	Bits 00–15 (00–17)	**Input Channel 0 input data** – Real time input data per your configuration
Word 1	Bits 00–15 (00–17)	**Input Channel 1 input data –** Real time input data per your configuration
Word 2	Bits 00–15 (00–17)	**Read Back Output Channel 0 –** During normal operation, it is a copy of the output of channel 0. During an EN transition, it is the condition of the output as determined by S1 and S0. **Note:** Read back data is an image of what the user has sent as output to the module; no checks are performed on the data.
Word 3	Bits 00–15 (00–17)	**Read Back Output Channel 1 –** During normal operation, it is a copy of the output of channel 1. During an EN transition, it is the condition of the output as determined by S1 and S0. **Note:** Read back data is an image of what the user has sent as output to the module; no checks are performed on the data.

Table 6.8
Word/Bit Descriptions for the 1794-IF2XOF2I Isolated Analog Combo Module

Write Word	Decimal Bit (Octal Bit)	Definition
Word 4	Bits 00–15 (00–17)	**Real Time Sample**. The elapsed time in increments programmed by the real time sample interval.
Word 5	Bits 00	Reserved
	Bits 01	**Calibration Done bit (DN). –** This bit is set to 1 after a calibration cycle is completed.
	Bits 02	**Calibration Bad bit (BD). –** This bit is set to 1 if the channel calibration coefficients cannot be saved or read properly.
	Bits 03-07	Set to 0.
	Bits 08-11 (10-12)	Reserved
	Bit 12 (14)	Set to 0
	Bit 13 (15)	**Configuration mode bit (CF)** – This bit is set (1) when the configuration mode is selected (bit 15, word 6 in the block transfer write set to 1). When this bit is set (1), the module status indicator flashes.
	Bit 14 (16)	**Field Power Off bit (FP)** – This bit is set (1) when the 24V field power fails. When this bit is set (1), the module status indicator flashes.
	Bit 15 (17)	**Power Up (unconfigured state) bit (PU).** – This bit is set (1) when the configuration word is all zeroes (0) due to a reset (adapter power cycle or module insertion) or a cleared configuration word (all 0). When this bit is set (1), the module status indicator flashes.
Word 6	Bits 00-01	**Underrange bits (U). –** These bits are set (1) when the input channel is below a preset limit as defined by the configuration selected. U0 (bit 00) corresponds to input channel 0 and U1 (bit 01) corresponds to input channel 1. Refer to Table 4.15.
	Bits 02-03	**Wire-Off status bits. (W). –** These bits, when set (1), indicate the corresponding current output channel is open. W0 (bit 02) corresponds to channel 0, and W1 (bit 03) corresponds to channel 1.
	Bits 04-05	**Overrange bits (V). –** These bits are set (1) when the input channel is above a preset limit as defined by the configuration selected. Bit 04 corresponds to input channel 0 and bit 05 corresponds to input channel 1. Refer to Table 4.15.
	Bits 06-09 (06-11)	Not used. Set to 0.
	Bits 10-11 (12-13)	**Hold output bits (P). –** These bits are set (1) in response to Q0 or Q1 and a transition of the EN bit. When P0 or P1 is set (1), they indicate that the output is holding at the level in the readback data for the respective channel. These bits return to 0 when the output data matches the readback output data.
	Bits 12-15 (14-17)	Not used. Set to 0.
Output Word 1	Bits 00-12 (00-14)	Not used.
	Bits 13-14 (15-16)	**Safe State Source bits (S1/S0). –** Not used in ControlNet applications. Turn these bits off (i.e. set to 0).
	Bit 15 (17)	**Output enable bit (EN)** Set this bit off (0) for the configuration block. Set this bit on (1) for the output block.

Table 6.8
Word/Bit Descriptions for the 1794-IF2XOF2I Isolated Analog Combo Module

Write Word	Decimal Bit (Octal Bit)	Definition
Word 1	Bits 00-15 (00-17)	**Output Channel 0 data**
Word 2	Bits 00-15 (00-17)	**Output Channel 1 data**
Configuration Word 0	**Input Channels 0 and 1 Filter Selections**	
	Bits 00-01	Channel 0 Filter Setting
	Bits 04-07	Channel 1 Filter Setting
	Bits 08-15 (11-17)	Not used
Word 1	**Channel Configuration**	
	Bits 00-03	**Input Channel 0 Configuration**
	Bits 04-07	**Input Channel 1 Configuration**
	Bits 08-11 (10-13)	**Output Channel 0 Configuration**
	Bits 12-15 (14-17)	**Output Channel 1 Configuration**
Word 2	Bits 00-14 (00-16)	**Real Time Sample Interval –** Programs the interval of the real time sample. Can be varied from 0 to 30 seconds (30000 decimal). Resolution is in ms with granularity in 5ms steps. Refer to 55.
Word 3	Bits 00-03	**Channel calibration selection bit.** When this bit is set (1), the channel can be calibrated using the initiate calibration bit (IC). Bit 00 corresponds to input channel 0, bit 01 corresponds to input channel 1, it 02 corresponds to output channel 2, bit 03 corresponds to output channel 3
	Bit 04	**Gain/Offset selection bit (GO). –** When this bit is cleared, a 0 to 1 to 0 transition of the CK bit performs on offset calibration. When this bit is 1, the module is directed to do a gain calibration.
	Bit 05	**Calibration clock bit (CK). –** When this bit is set to 1 (calibration mode), the calibration coeffiicient for the selected channels is accepted. When this bit is reset (0), the accepted calibration coefficients for the selected channels are stored, applied, and the calibration mode exited. Monitor status bits DN and BD for succesful calibration.
	Bit 06	**Quick Calibration bit (QK). –** Normally reset (0). When this bit is set (1) during a calibration sequence, the calibration coefficient is stored to all related configurations for the selected channels. **NOTE:** This method of calibration quickly calibrates the selected channels, you will not be within the rated accuracy of the module.
	Bit 07	**Revert to defaults bit (RV). –** Normally reset (0). When set (1) during a calibration procedure, default values for selected channels are used for the calibration coefficient. **NOTE:** You will not be within the rated accuracy of the module.
	Bits 08-09 (10-11)	Not used. Set to 0.

Table 6.8
Word/Bit Descriptions for the 1794-IF2XOF2I Isolated Analog Combo Module

Write Word	Decimal Bit (Octal Bit)	Definition
Word 3	Bits 10-11 (12-13)	**Request for hold outputs (Q). –** Channel request bits that instruct an output to hold its output level when EN transitions from 0 to 1 to 0. When EN is 0, outputs go to a safe state dictated by S1/S0. When EN returns to 1, the outputs will hold their level until the output data equals the output level. P0–P3 indicates channels holding. Output read back data shows what level is being held. Q0 = bit 08 (10) = channel 0; Q1 = bit 08 (10) = channel 1, etc.
	Bit 12 (14)	**Interrupt Toggle bit (IT) –** This bit, when set (1), permits interleaving of module interrupts ensuring exchange of critical data when channels are configured for their fastest update times. RTSI and "no low pass filter" must be 0 in order for the module to recognize this feature. This groups data update rates for all channels to the slowest configuration setting of any of the channels. In addition, channel update rates for all channels with a 7.5ms update rate are reduced to 5.0ms. When reset (0), real time sampling and filter features are enabled.
	Bit 13 (15)	**Transparent bit (TR). –** This bit, when set to 1, permits configuration to be changed without using the IC bit.
	Bit 15 (17)	**Initiate Configuration bit (IC). –** When set (1), instructs the module to enter configuration mode. Present configuration data prior to or coincident with IC being set. Once IC returns to 0, additional configuration information is ignored.
Word 4	Bits 00-12 (00-14)	Not used.
	Bits 13-14 (15-16)	**Safe State Source bits (S1/S0). –**Not used in ControlNet applications. Set these bits off (0).
	Bit 15 (17)	**Output enable bit (EN)** Set this bit off (0) for the configuration block. Set this bit on (1) for the output block.
Word 5	Bits 00-15 (00-17)	Output Channel 0 data.
Word 6	Bits 00-15 (00-17)	Output Channel 1 data.

Table 6.9
Configuring Your Input Channels

Input Channel Configuration									
03	02	01	00	Set these bits for Channel 0					
07	06	05	04	Set these bits for Channel 1					
Bit Settings				**Input Values**	**Data Format**	**% Underrange %Overrange**	**Input Range**		**Module Update Rate**
							Hexadecimal	**Decimal**	**(RTS = 0)**
0	0	0	0	Channel not configured					
0	0	0	1	4–20mA	signed 2's complement	4% Under; 4% Over	<0000–7878>	<0000–30840>	7.5ms
0	0	1	0	±10V	signed 2's complement	2% Under, 2% Over	<831F–7CE1>	<–31969–31969>	2.5ms
0	0	1	1	±5V	signed 2's complement	4% Under, 4% Over	<8618–79E8>	<–31208–31208>	2.5ms
0	1	0	0	0–20mA	signed 2's complement %	0% Under, 4% Over	0–10000>	0–10000>	7.5ms

Table 6.9
Configuring Your Input Channels

0	1	0	1	4-20mA	signed 2's complement %	4% Under, 4% Over	<0–10000>	<0–10000>	7.5ms
0	1	1	0	0–10V	signed 2's complement %	0% Under, 2% Over	0–10000>	0–10000>	5.0ms
0	1	1	1	±10V	signed 2's complement %	2% Under, 2% Over	<–10000–10000>	<–10000–10000>	5.0ms
1	0	0	0	0–20mA	binary	0% Under, 4% Over	0000–F3CF>	0000–62415>	2.5ms
1	0	0	1	4–20mA[1]	binary	4% Under, 4% Over	0000–F0F1>	0000–61681>	7.5ms
1	0	1	0	0–10V	binary	0% Under, 2% Over	0000–F9C2>	0000–62415>	2.5ms
1	0	1	1	0–5V	binary	0% Under, 4% Over	0000–F3CF>	0000–62415>	2.5ms
1	1	0	0	±20mA	offset binary, 8000H = 0mA	4% Under, 4% Over	<0618–F9E8>	<32768–63976>	2.5ms
1	1	0	1	4–20mA	offset binary, 8000H = 4mA	4% Under, 4% Over	<8000–F878>	<32768–63608>	7.5ms
1	1	1	0	±10V	offset binary, 8000H = 0V	2% Under, 2% Over	<031F–FCE1>	<1560–63976>	2.5ms
1	1	1	1	+5V	offset binary, 8000H = 0V	4% Under, 4% Over	<0618–F9E8>	<1560–63976>	2.5ms

(1) Underrange for 4-20mA occurs in the blind area below 0 (3.2mA).

Table 6.10
Setting the Input Filter

Bits				**Channel**	
03	02	01	00	Input Channel 0	
07	06	05	04	Input Channel 1	
				A/D Conversion Rate	**Low Pass Filter**
0	0	0	0	1200Hz	No low pass
0	0	0	1	1200Hz	100ms low pass
0	0	1	0	1200Hz	500ms low pass
0	0	1	1	1200Hz	1000ms low pass
0	1	0	0	600Hz	No low pass
0	1	0	1	600Hz	100ms low pass
0	1	1	0	600Hz	500ms low pass
0	1	1	1	600Hz	1000ms low pass
1	0	0	0	300Hz	No low pass
1	0	0	1	300Hz	100ms low pass
1	0	1	0	300Hz	500ms low pass
1	0	1	1	300Hz	1000ms low pass
1	1	0	0	150Hz	No low pass
1	1	0	1	150Hz	100ms low pass
1	1	1	0	150Hz	500ms low pass
1	1	1	1	150Hz	1000ms low pass

Table 6.11
Configuring Your Outputs for the 1794-IF2XOF2I Analog Combo Module

Configuration Bits				Nominal Range	Data Type	Output Values[1]		Update Rate
MSD		LSD				Hexadecimal	Decimal	
0	0	0	1	4-20mA	2's complement	<0000–7878>	<0000–30840>	5.0ms
0	0	1	0	±10V	2's complement	<8618–79E8>	<–31208–31208>	2.5ms
0	0	1	1	±5V	2's complement	<8618–79E8>	<–31208–31208>	2.5ms
0	1	0	0	0-20mA	2's complement %	0–10000>	0–10000>	5.0ms
0	1	0	1	4-20mA	2's complement %	<0–10000>	<0–10000>	5.0ms
0	1	1	0	0-10V	2's complement %	0–10000>	0–10000>	5.0ms
0	1	1	1	±10V	2's complement	<–10000-10000>	<–10000–10000>	5.0ms
1	0	0	0	0-20mA	binary	0000–F3CF>	0000–62415>	2.5ms
1	0	0	1	4-20mA	binary	0000–F0F1>	0000–61681>	5.0ms
1	0	1	0	0–10V	binary	0000–F3CF>	0000–62415>	2.5ms
1	0	1	1	0-5V	binary	0000–F3CF>	0000–62415>	2.5ms
1	1	0	0	±20mA	offset binary	8000–F9E8>	32768–63976>	2.5ms
1	1	0	1	4-20mA	offset binary	<8000–F878>	<32768–63608>	5.0ms
1	1	1	0	±10V	offset binary	<0618–F9E8>	<1560–63976>	2.5ms
1	1	1	1	±5V	offset binary	<0618–F9E8>	<1560–63976>	2.5ms

(1) < and > indicate the overrun beyond actual range (about 5%).

Calibrating Your Module

Chapter Objective

In this chapter we tell you:

- what tools are needed to calibrate
- how to calibrate your module
- how to scale to engineering units

When and How to Calibrate Your Isolated Analog Module

Your module is shipped to you already calibrated for 150Hz, 300Hz and 600Hz. If you are checking calibration, or if it becomes necessary to recalibrate the module, you must do so with the module in a FLEX I/O system. The module must communicate with the processor and industrial terminal.

Before calibrating the module, if ladder logic is used for calibration rather than the GUI available for the IF4I and IF2XOF2I modules, you must enter ladder logic into the processor memory, so that you can initiate BTWs to the module, and the processor can read inputs from the module.

Periodically (frequency based on your application), check your module calibration. Calibration may be required to remove module error due to aging of components in your system.

Calibration can be accomplished using any of three methods:

- manual calibration, as described below.
- 6200 I/O CONFIGURATION software – refer to your 6200 software publications for procedures for calibrating.
- RSLogix GUI available for the IF2XOF2I and IF4I with an EtherNet IP or ControlNet adapter. RSLogix guides the user through the process sequentially with no need for use of block transfers.

When calibrating your module, you must perform:

- Input and output module (in voltage mode) – offset calibration first, gain calibration second
- Output module (in current mode) – gain calibration first, offset calibration second, and another gain calibration third.

Tools and Equipment

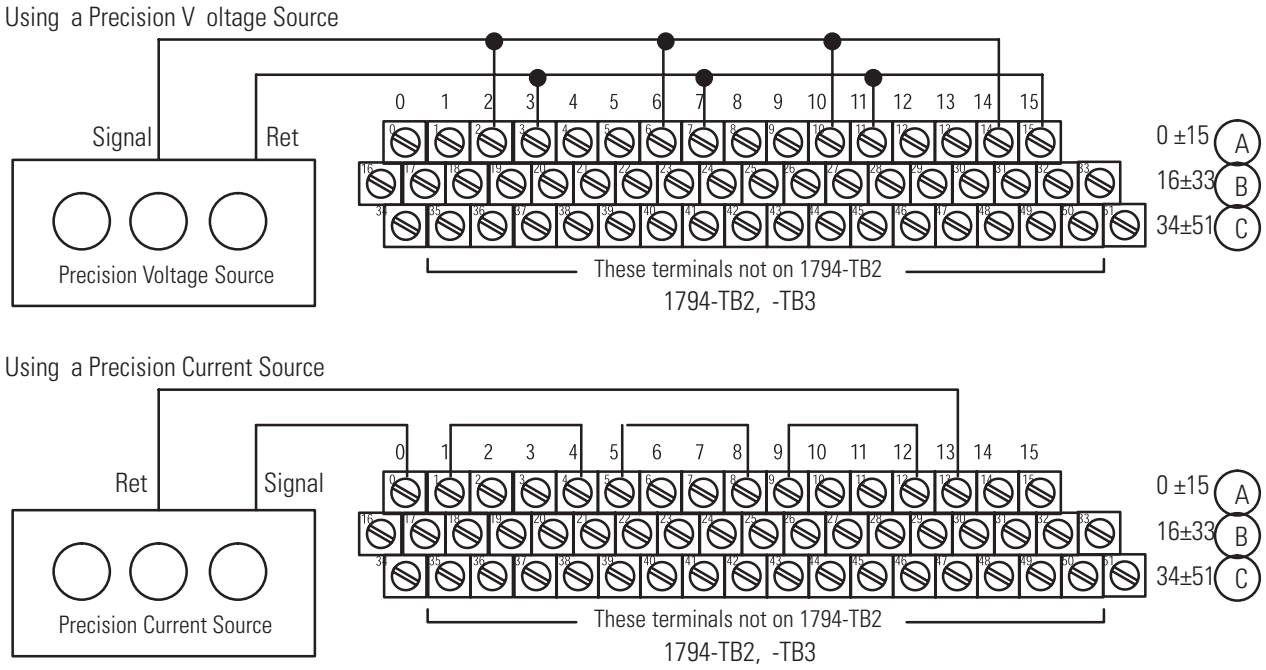
In order to calibrate your input module you will need the following tools and equipment:

Tool or Equipment	Description	Model/Type	Available From:
Precision Voltage/Current Source	0–10.25V, 10µV resolution or better 0–21mA, 100nA or better	HP3245A or equivalent	
Precision Voltage/Current Meter	0–10.5V, 10µV or better 0–22mA, 100nA or better	Datron, Wavetek or equivalent	
Industrial Terminal and Interconnect Cable	Programming terminal for A–B family processors	Cat. No. 1770–T3 or Cat. No. 1784–T45, –T47, –T50, etc.	Allen–Bradley Company Highland Heights, OH

ATTENTION

The isolated analog modules are shipped **already calibrated for 150Hz, 300Hz and 600Hz.** No recalibration is required when switching between these conversion rates.

Figure 7.1
Calibration Set-Ups



Calibrating Your Isolated Analog Input Module

The analog input module is shipped **already calibrated for 150Hz, 300Hz and 600Hz.** No recalibration is required when switching between these conversion rates. Recalibration is required when going to 1200Hz conversion rate. Calibration of the module consists of applying a voltage or current across each input channel for offset and gain calibration.

Bits Used During Calibration

Refer to chapter 4 for bit/word descriptions. The following bits are used during calibration of your module:

IC = initiate configuration. This bit must be set (1) to initiate calibration

RV = revert to defaults. When this bit is set (1) during a calibration sequence, default values for the selected channels are used for the calibration coefficients. This bit normally reset (0).

QK = quick calibration. When this bit is set (1) during a calibration sequence, the calibration coefficient is stored to all related configurations for the selected channels. For example, if a calibration is performed in a voltage mode, QK allows the calibration coefficient to be stored to all voltage modes. This bit is normally reset (0).

CK = calibration clock. When this bit is set to 1, calibration mode starts and calibration coefficients for the selected channels are accepted. When cleared to 0, the accepted current calibration coefficients are stored to the selected channels, applied and calibration mode exited. Monitor status bits DN and BD of success of calibration.

GO = gain/offset select. When this bit is set to 1, a 0 to 1 to 0 transition pattern of the CK bit causes a gain calibration to be performed. When this bit is cleared to 0, a 0 to 1 to 0 transition pattern of the CK bit caused an offset calibration to be performed.

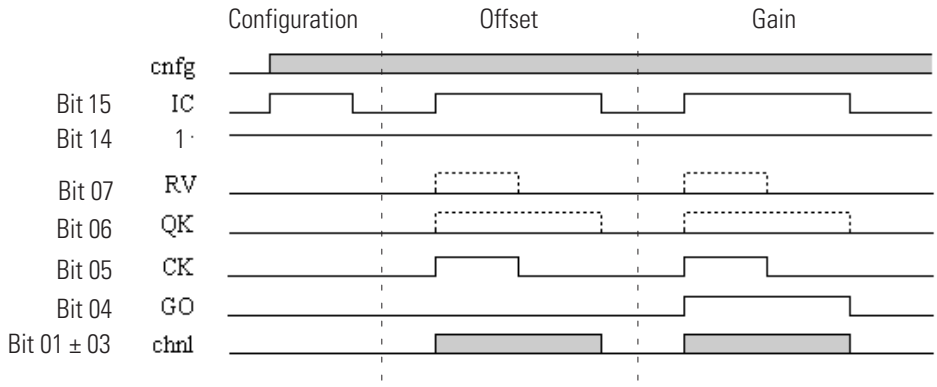
Offset Calibration for Inputs

Refer to the input timing diagram when calibrating the module. Normally all inputs are calibrated together. To calibrate the offset, proceed as follows:

1. The module must be calibrated in an operating system. Connect your module in a calibration setup as shown above.

2. Send a block transfer write (BTW) to the module with individual channel bits set for the configuration desired for each input. This effectively terminates any previous configuration of the module/channel.

Figure 7.2
Input Calibration Timing Diagram



3. Apply offset voltage (0V) or current (0mA) to the input(s) to be configured.

4. Send a block transfer write to set the IC bit and CK bit (1), and reset the GO bit (0). This tells the module to determine offset coefficients for the selected channels.

   If you also set the RV bit to 1, the default values are assigned to each channel. The default values are near but not precisely on the calibration mark.

5. Send another BTW to the module to reset the CK bit (0). When the GO bit is low, the previously determined offset coefficients are stored in EEPROM for the selected channels. If QK is set (1) high, the same coefficients will be stored to all "like" configurations (i.e. if configuration bits are set for a specific voltage, both unipolar/bipolar, x1/x2 – will have the same coefficients stored – see Table 7.1). If calibrate for 0-20mA current range, 4-20mA range channels are also automatically calibrated.

Table 7.1

Configuration	Nominal Range	Data Type	Comments
4	0–20mA	signed 2's complement %	If you calibrate any of this group, the rest of the group will also be calibrated.
8	0–20mA	binary	
C	±20mA	offset binary	
6	0–10V	signed 2's complement %	If you calibrate any of this group, the rest of the group will also be calibrated.
A	0–10V	binary	
B	0–5V	binary	
2	±10V	signed 2's complement	If you calibrate any of this group, the rest of the group will also be calibrated.
7	±10V	signed 2's complement %	
E	±10V	offset binary	
3	±5V	signed 2's complement	If you calibrate any of this group, the rest of the group will also be calibrated.
F	±5V	offset binary	
1	4–20mA	signed 2's complement	If you calibrate 0-20mA range, all 4- mA g s are calibrated.
5	4-20mA	signed 2's complement %	
9	4–20mA	binary	
D	4–20mA	offset binary	

6. Monitor the module block transfer read word. Clear the IC bit to 0, and offset calibration is terminated.

Setting the Input Gain

Set the gain of the module second. You must set the offset before setting the gain.

1. Apply gain voltage (5.25V or 10.25V) or current (21.0mA) toselected inputs.

2. Send a BTW to the module to set the IC bit and the CK bit to 1 and the GO bit to 1. This tells the module to determine gain voltage/current for the selected channels. If you also set the RV bit to 1, default values will be used on all selected channels.

3. Send a BTW to the module to reset the CK bit to 0 with the GO bit still 1. This stores previously determined coefficients into EEPROM on selected channels. If QK is set (1), the same coefficients will be stored to all “like” configurations. For example, if configuration is set to voltage, bipolar/polar, X1/X2 will also be configured. See the table on the previous page.

4. Monitor the module block transfer read word. Clear the IC bit. Gain calibration is terminated.

Calibrating Your Isolated Analog Output Module

Calibration of the module consists of measuring a voltage or current across each output, and calculating an offset or gain correction value.

IMPORTANT Voltage calibration requires offset calibration followed by gain calibration. Current calibration requires gain calibration followed by offset calibration, and then a limited gain calibration using corrected coefficients.

Bits Used During Calibration

Refer to chapter 4 for bit/word descriptions. The following bits are used during calibration of your module:

IC = initiate configuration. This bit must be set (1) to initiate calibration

RV = revert to defaults. When this bit is set (1) during a calibration sequence, default values for the selected channels are used for the calibration coefficients. This bit normally reset (0).

QK = quick calibration. When this bit is set (1) during a calibration sequence, the calibration coefficient is stored to all related configurations for the selected channels. For example, if a calibration is performed in a voltage mode, QK allows the calibration coefficient to be stored to all voltage modes.

CK = calibration clock. When this bit is set to 1, calibration mode starts and calibration coefficients for the selected channels are accepted. When cleared to 0, the accepted current calibration coefficients are stored to the selected channels, applied and calibration mode exited. Monitor status bits DN and BD of success of calibration.

GO = gain/offset select. When this bit is set to 1, a 0 to 1 to 0 transition pattern of the CK bit causes a gain calibration to be performed. When this bit is cleared to 0, a 0 to 1 to 0 transition pattern of the CK bit caused an offset calibration to be performed.

Calibrating Voltage Outputs

Voltage calibration requires offset calibration followed by gain calibration.

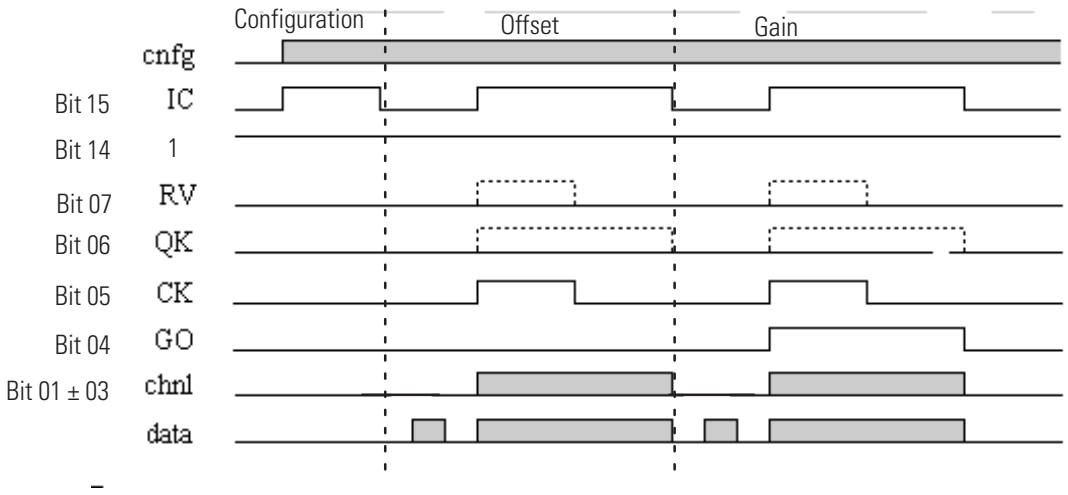
Offset Calibration for Voltage Outputs

Refer to the output timing diagram when calibrating the module. Normally all outputs are calibrated together. To calibrate the offset of an output, proceed as follows:

1. If you are not calibrating all channels with the same configuration, select the channel to be calibrated by setting the bit for that channel.

2. Send a block transfer write (BTW) to the module with individual channel bits set for the configuration desired for each output. This effectively terminates any previous configuration of the module/channel.

Figure 7.3
Output Calibration Timing Diagram



3. Clear all offset and gain coefficients by :
   a. Set output data to 0 and the IC bit to 1
   b. With GO = 0, toggle the CK bit
   c. With GO = 1, toggle the CK bit
   d. Clear the IC bit

4. Send a block transfer write with the output values for offset voltage to the module (–31208 for –10V mode 2). Measure the output.

   Calculate the offset correction for each channel:

   offset_corr = (–10V – measured_value) X 3120.7619

5. Enter these offset corrections in the output word for each channel being calibrated.

6. Send a block transfer write with the IC bit and the CK bit set to 1. With GO low (0), the module copies the "offset_corr" coefficients (signed 2's complement format) from the data words into offset storage for the selected channels. If you set RV high (1), default values will be copied to all channels.

7. With a BTW, reset the CK bit (0). With the GO bit low (0), the previously determined offset coefficients are stored in EEPROM for the selected channel.

8. Monitor the block transfer read. Clear the IC bit to 0. Offset calibration is completed.

Gain Calibration for Outputs

1. Send a block transfer write to the module to set the output values for gain voltage; +31208 for +10V mode 2. Measure the output. Calculate the gain correction for each channel as follows:

   gain_corr = (+10V – measured_value) X 3276.76

2. Enter these gain corrections in the output word for each channel being calibrated.

3. Send a block transfer write with the CK bit set to 1. With GO high, the module will copy "gain_corr" coefficients (signed 2's complement format) from the data words into gain storage for the selected channels. If RV is high, default values will be copied to all channels.

4. Send a block transfer write with CK set to 0. With GO high, the previously determined gain coefficients are stored into EEPROM as directed by the channel selection.

5. Clear the IC bit to 0. Gain calibration is terminated.

Calibrating Current Outputs

Current calibration requires gain calibration followed by offset calibration, and a limited gain calibration using corrected coefficients.

Gain Calibration for Current Outputs

1. Send a block transfer write to the module to set the output values for gain voltage; F3CF hex for 20.0mA mode 8. Measure the output. Calculate the gain correction for each channel as follows:

   gain_corr = (0.02A – measured_value) X 3202194.613

2. Enter these gain corrections in the output word for each channel being calibrated. Record each of the values to be used later.

3. Send a block transfer write with the CK bit set to 1. With GO high, the module will copy “gain_corr” coefficients (signed 2’s complement format) from the data words into gain storage for the selected channels. If RV is high, default values will be copied to all channels.

4. Send a block transfer write with CK set to 0. With GO high, the previously determined gain coefficients are stored into EEPROM as directed by the channel selection.

5. Clear the IC bit to 0. Gain calibration is terminated.

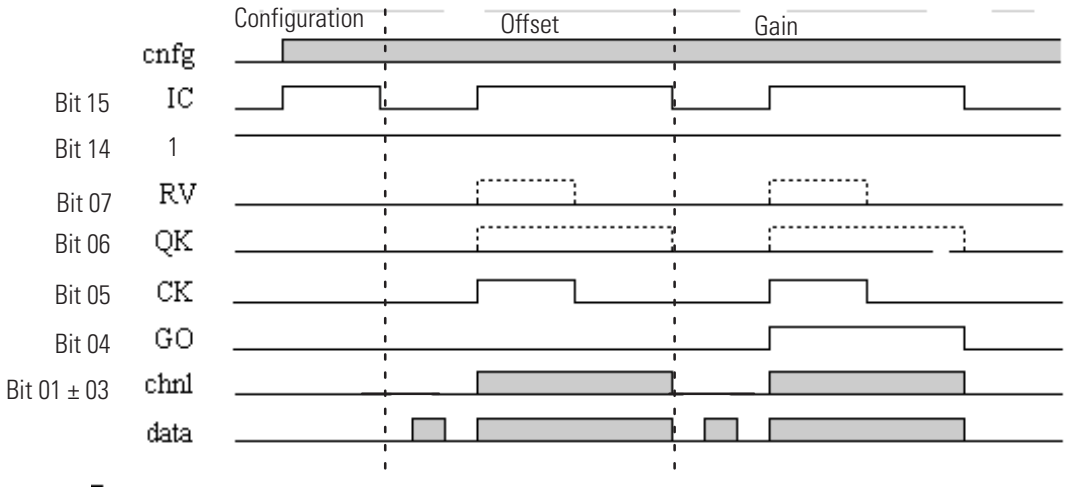
Offset Calibration for Current Outputs

Refer to the output timing diagram when calibrating the module. Normally all outputs are calibrated together. To calibrate the offset of an output, proceed as follows:

1. If you are not calibrating all channels with the same configuration, select the channel to be calibrated by setting the bit for that channel.

2. Send a block transfer write (BTW) to the module with individual channel bits set for the configuration desired for each output. This effectively terminates any previous configuration of the module/channel.

Figure 7.4
Output Calibration Timing Diagram



3. Clear all offset and gain coefficients by:
   a. Set output data to 0 and the IC bit to 1
   b. With GO = 0, toggle the CK bit
   c. With GO = 1, toggle the CK bit
   d. Clear the IC bit

4. Send a block transfer write with the output values for offset voltage to the module (+1560 for 0.5mA mode 8). Measure the output.

   Calculate the offset correction for each channel as follows:

   offset_corr = (0.0005 – measured_value) X 1524873.192

5. Enter these offset corrections in the output word for each channel being calibrated. Record each of the values to be used later.

6. Send a block transfer write with the IC bit and the CK bit set to 1. With GO low (0), the module copies the "offset_corr" coefficients (signed 2's complement format) from the data words into offset storage for the selected channels. If you set RV high (1), default values will be copied to all channels.

7. With a BTW, reset the CK bit (0). With the GO bit low (0), the previously determined offset coefficients are stored in EEPROM for the selected channel.

8. Monitor the block transfer read. Clear the IC bit to 0. Offset calibration is completed. Proceed with final gain calibration.

Final Gain Calibration for Current Inputs

After performing a gain calibration and an offset calibration:

1. Enter a new gain correction calculated as follows into the respective output words:

   new gain_corr = gain_corr – (2 x offset_corr)

2. Send a block transfer write with the CK bit set to 1. With GO high, the module will copy “gain_corr” coefficients (signed 2’s complement format) from the data words into gain storage for the selected channels. If RV is high, default values will be copied to all channels.

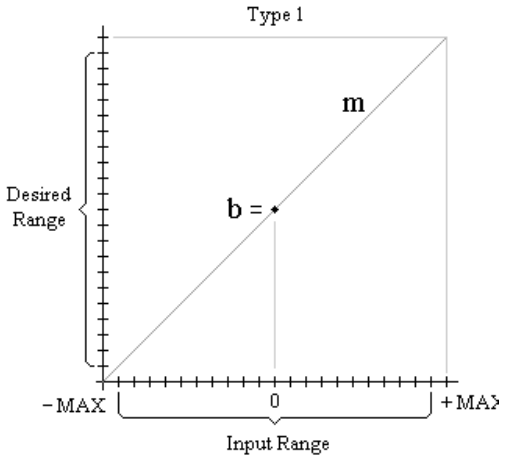
3. Send a block transfer write with CK set to 0. With GO high, the previously determined gain coefficients are stored into EEPROM as directed by the channel selection.

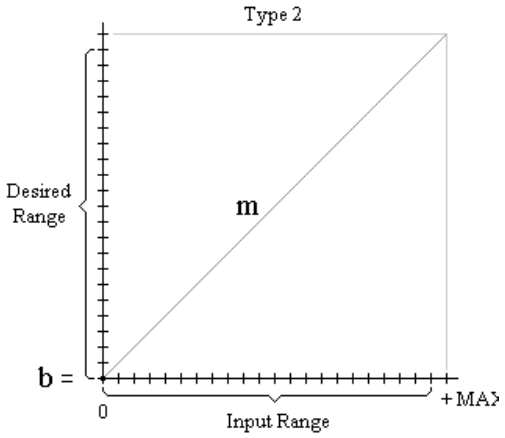
4. Clear the IC bit to 0. Gain calibration is terminated.

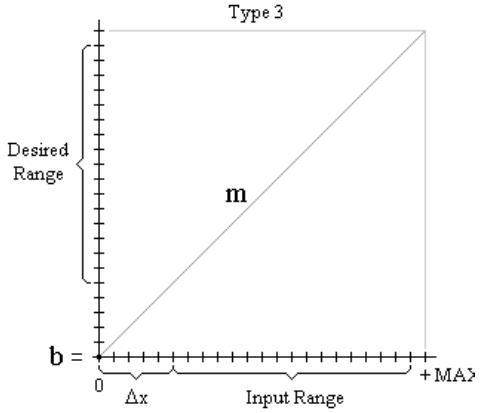
Scaling Inputs

Inputs are scaled using the y = mx + b linear formula, as illustrated by the three types below.

Configu-ration	Nominal Range	Data Type	Scale Figure	Output Range	ΔX
1	4–20mA	signed 2's complement	Type 2	30840	NA
2	±10V	signed 2's complement	Type 1	63938	NA
3	±5V	signed 2's complement	Type 1	62416	NA
4	0–20mA	signed 2's complement %	Type 2	10000	NA
5	4-20mA	signed 2's complement %	Type 2	10000	NA
6	0–10V	signed 2's complement %	Type 2	10000	NA
7	±10V	signed 2's complement %	Type 1	20000	NA
8	0–20mA	binary	Type 2	62415	NA
9	4–20mA	binary	Type 2	61681	NA
A	0–10V	binary	Type 2	63938	NA
B	0–5V	binary	Type 2	62415	NA
C	±20mA	offset binary	Type 3	62416	1560
D	4–20mA	offset binary	Type 3	30840	32768
E	±10V	offset binary	Type 3	63938	799
F	±5V	offset binary	Type 3	62416	1560







The gain, m, and offset, b, coefficients are calculated as follows:

m = Desired Range / Input Range

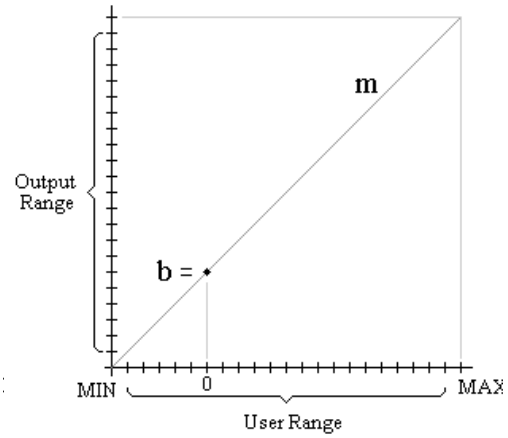
b = Desired value when input returns zero (type 1 & 2)

b = – m(Δx) + (bottom of Desired Range) (type 3)

Scaling Outputs

Outputs are scaled in the same manner as the inputs and are represented by the following illustration.

Configu-ration	Nominal Range	Data Type	Output Range	Z
1	4–20mA	signed 2's complement	30840	0
2	±10V	signed 2's complement	62416	0
3	±5V	signed 2's complement	62416	0
4	0–20mA	signed 2's complement %	10000	0
5	4-20mA	signed 2's complement %	10000	0
6	0–10V	signed 2's complement %	10000	0
7	±10V	signed 2's complement %	20000	0
8	0–20mA	binary	62415	0
9	4–20mA	binary	61681	0
A	0–10V	binary	62415	0
B	0–5V	binary	62415	0
C	±20mA	offset binary	31208	32768
D	4–20mA	offset binary	30840	32768
E	±10V	offset binary	62416	32768
F	±5V	offset binary	62416	32768



The gain, m, and offset, b, coefficients are calculated as follows:

m = Output Range / User Range

b = **Z** – mx

where: **Z** is the value, from the table, that sends a "zero" output*,

x0 is the user signal that is associated with "zero" output.

* in 4–20mA modes, "zero" is 4mA.

Chapter Summary

In this chapter, you learned how to calibrate your isolated analog module.

Specifications

Specifications for the modules, including environmental and certifications can be found in the following Installation Instructions.

Catalogs	Publication
1794-OF4I	1794-IN037
1794-IF4I	1794-IN038
1794-IF2XOF2I	1794-IN039
1794-IF4IXT, 1794-OF4IXT, 1794-IF2XOF2IXT	1794-IN129
1794-IF4ICFXT	1794-IN130

Filter Response for 150Hz, 300Hz and 600Hz Conversion

Figure A.1
Filter Response at 150Hz Conversion

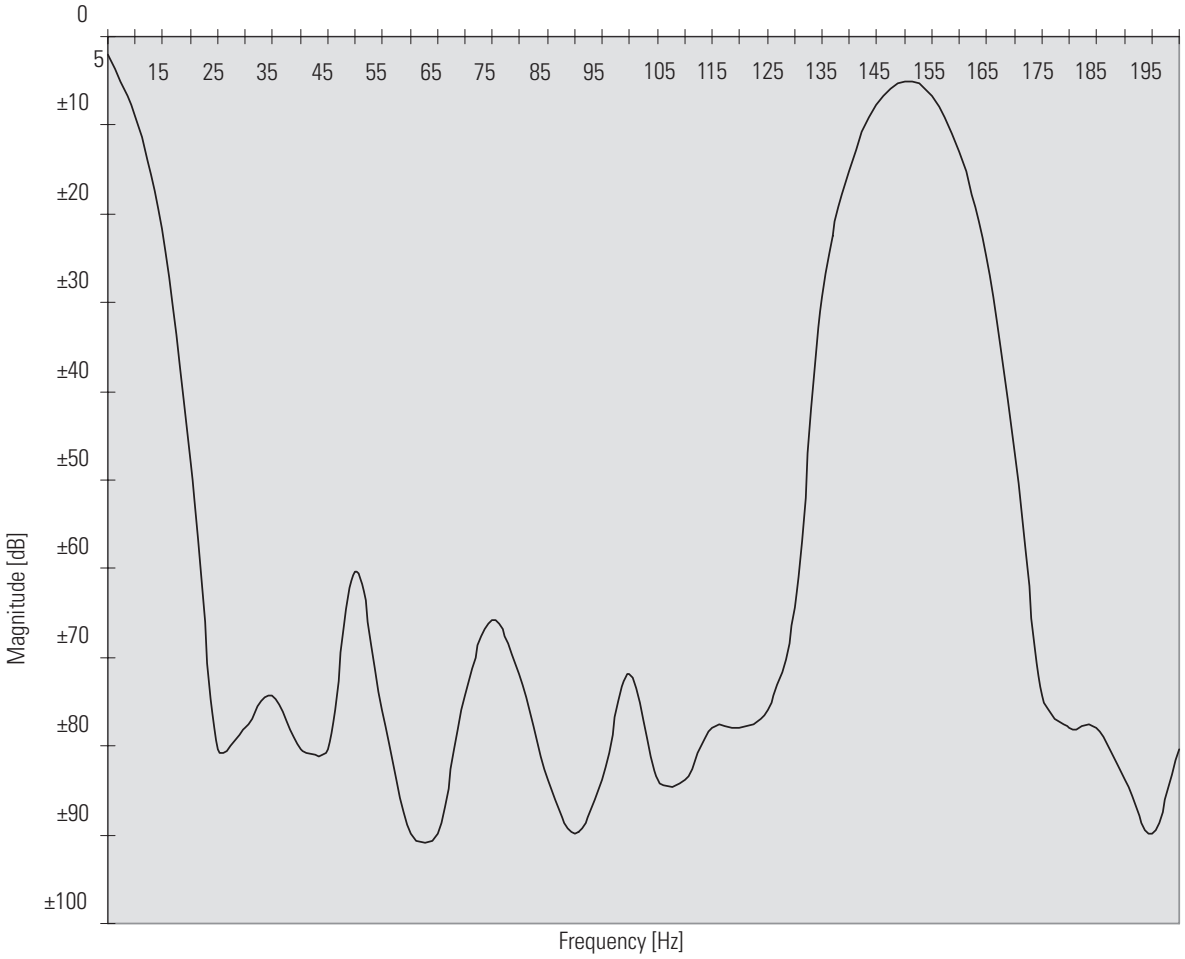


Figure A.2
Filter Response at 300Hz Conversion

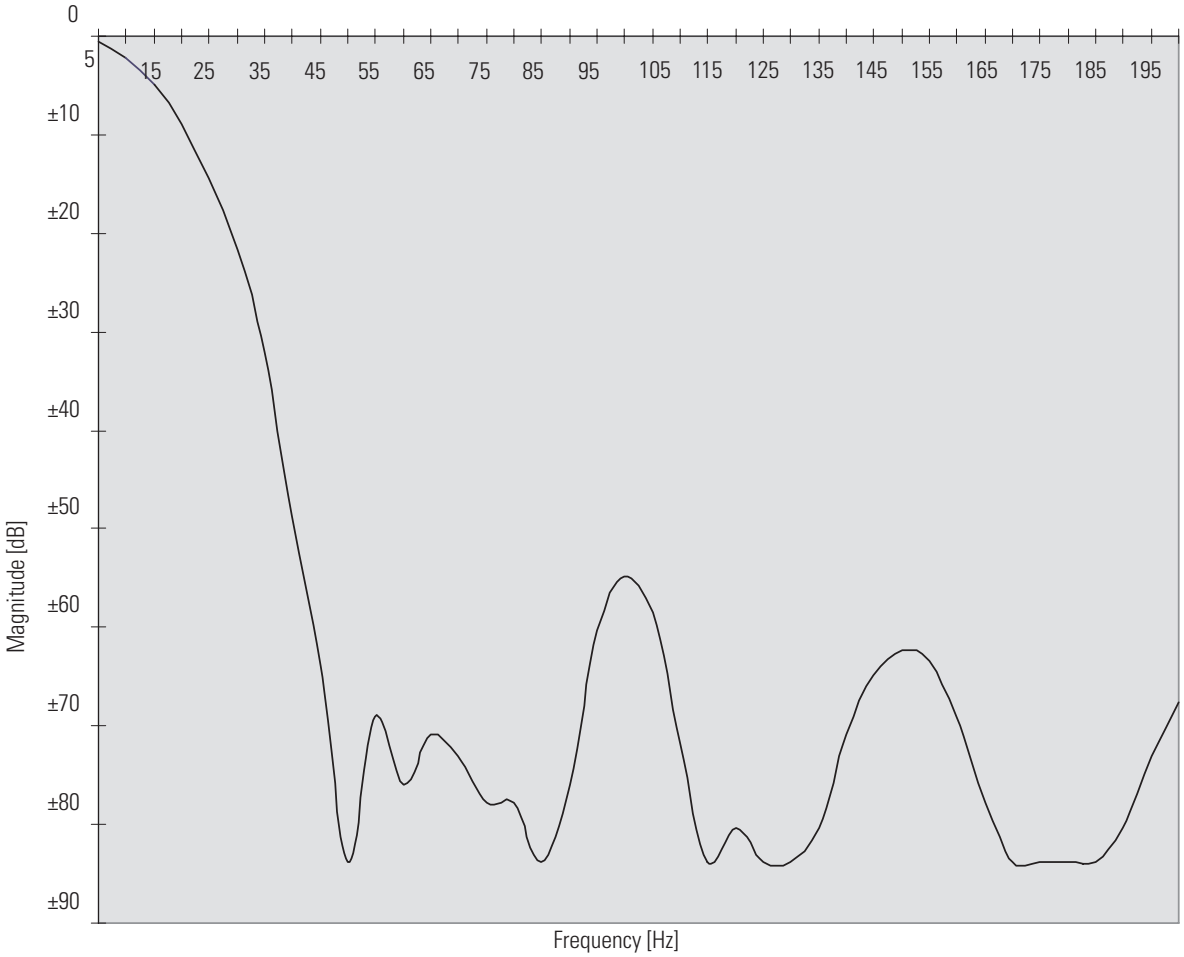
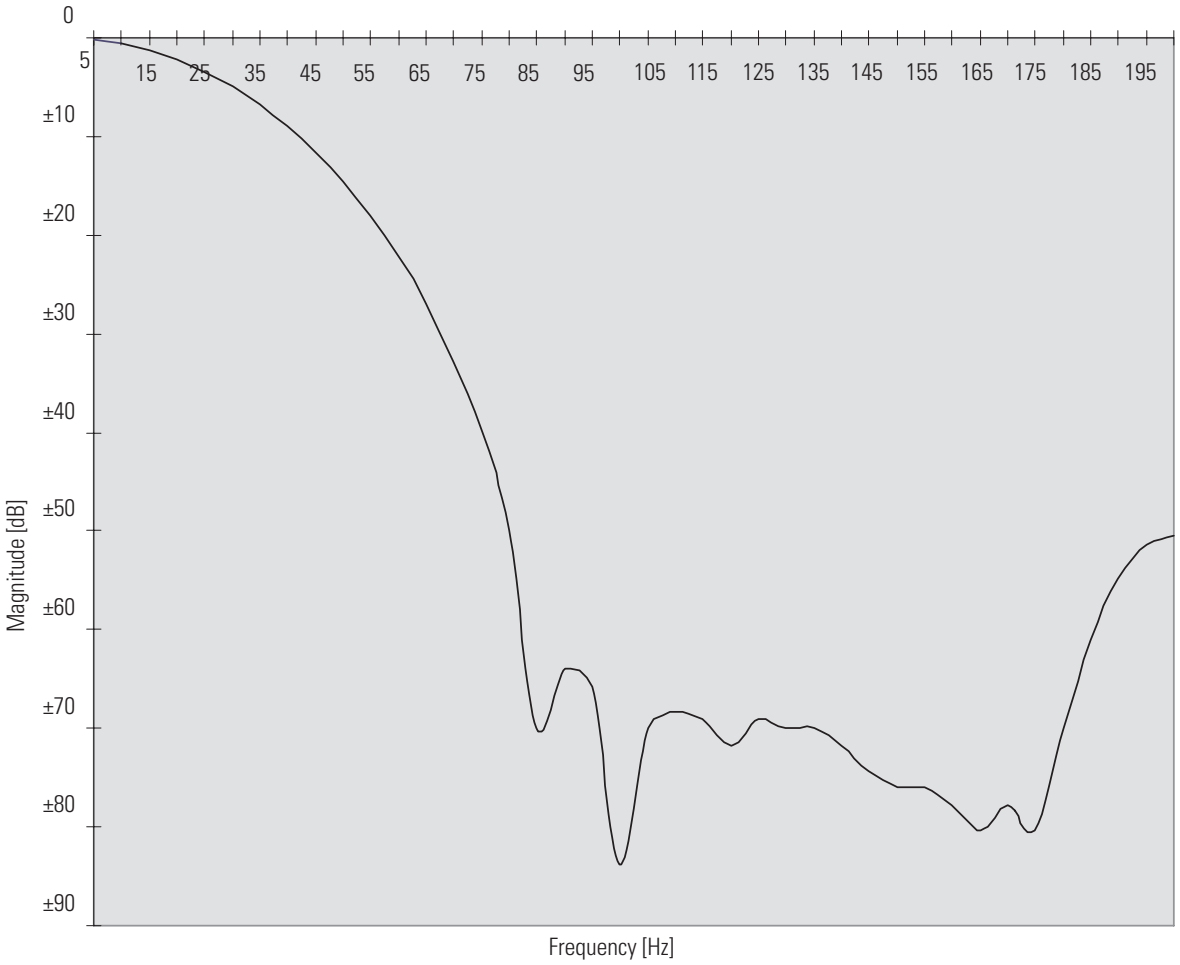


Figure A.3
Filter Response at 600Hz Conversion



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The following information applies when operating this equipment in hazardous locations:	**Informations sur l'utilisation de cet équipement en environnements dangereux :**
Products marked "CL I, DIV 2, GP A, B, C, D" are suitable for use in Class I Division 2 Groups A, B, C, D, Hazardous Locations and nonhazardous locations only. Each product is supplied with markings on the rating nameplate indicating the hazardous location temperature code. When combining products within a system, the most adverse temperature code (lowest "T" number) may be used to help determine the overall temperature code of the system. Combinations of equipment in your system are subject to investigation by the local Authority Having Jurisdiction at the time of installation.	Les produits marqués "CL I, DIV 2, GP A, B, C, D" ne conviennent qu'à une utilisation en environnements de Classe I Division 2 Groupes A, B, C, D dangereux et non dangereux. Chaque produit est livré avec des marquages sur sa plaque d'identification qui indiquent le code de température pour les environnements dangereux. Lorsque plusieurs produits sont combinés dans un système, le code de température le plus défavorable (code de température le plus faible) peut être utilisé pour déterminer le code de température global du système. Les combinaisons d'équipements dans le système sont sujettes à inspection par les autorités locales qualifiées au moment de l'installation.

WARNING	**EXPLOSION HAZARD**	**AVERTISSEMENT**	**RISQUE D'EXPLOSION**
	• Do not disconnect equipment unless power has been removed or the area is known to be nonhazardous. • Do not disconnect connections to this equipment unless power has been removed or the area is known to be nonhazardous. Secure any external connections that mate to this equipment by using screws, sliding latches, threaded connectors, or other means provided with this product. • Substitution of components may impair suitability for Class I, Division 2. • If this product contains batteries, they must only be changed in an area known to be nonhazardous.		• Couper le courant ou s'assurer que l'environnement est classé non dangereux avant de débrancher l'équipement. • Couper le courant ou s'assurer que l'environnement est classé non dangereux avant de débrancher les connecteurs. Fixer tous les connecteurs externes reliés à cet équipement à l'aide de vis, loquets coulissants, connecteurs filetés ou autres moyens fournis avec ce produit. • La substitution de composants peut rendre cet équipement inadapté à une utilisation en environnement de Classe I, Division 2. • S'assurer que l'environnement est classé non dangereux avant de changer les piles.

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