Allen-Bradley

Multi-Channel High Speed Counter

(Catalog Number 1746-HSCE2)

User Manual

Rockwell Automation

Important User Information

Because of the variety of uses for the products described in this publication, those responsible for the application and use of these products must satisfy themselves that all necessary steps have been taken to assure that each application and use meets all performance and safety requirements, including any applicable laws, regulations, codes and standards. In no event will Rockwell Automation be responsible or liable for indirect or consequential damage resulting from the use or application of these products.

Any illustrations, charts, sample programs, and layout examples shown in this publication are intended solely for purposes of example. Since there are many variables and requirements associated with any particular installation, Rockwell Automation does not assume responsibility or liability (to include intellectual property liability) for actual use based upon the examples shown in this publication.

Allen-Bradley publication SGI-1.1, *Safety Guidelines for the Application, Installation and Maintenance of Solid-State Control* (available from your local Rockwell Automation office), describes some important differences between solid-state equipment and electromechanical devices that should be taken into consideration when applying products such as those described in this publication.

Throughout this publication, notes may be used to make you aware of safety considerations. The following annotations and their accompanying statements help you to identify a potential hazard, avoid a potential hazard, and recognize the consequences of a potential hazard:

WARNING

Identifies information about practices or circumstances that can cause an explosion in a hazardous environment, which may lead to personal injury or death, property damage, or economic loss.

ATTENTION

Identifies information about practices or circumstances that can lead to personal injury or death, property damage, or economic loss.

IMPORTANT

Identifies information that is critical for successful application and understanding of the product.

The information below summarizes the changes to this manual since the last printing.

To help you find new information and updated information in this release of the manual, we have included change bars as shown to the right of this paragraph.

New Information

The table below lists sections that include new information.

For this new information	See page(s)
Note on limitations of rate value calculation at input frequencies below 60 Hz.	2-11
Clarified operation of Module Fault (MFLT) bit	2-17
Updated resistor information in single-ended wiring diagrams	3-9 and 3-10
Clarified programming cycle	4-2
Modifications to the COP instruction example for reading and writing floating point data	4-4
Corrected bit identification in Output State Byte	4-22
Example showing how to activate debug mode	5-10
Corrected bit identification table for Program Ranges Block	C-2

Read this preface to familiarize yourself with the rest of the manual. This preface covers the following topics:

- who should use this manual
- how to use this manual
- related publications
- conventions used in this manual
- Rockwell Automation support

Who Should Use This Manual

Use this manual if you are responsible for designing, installing, programming, or troubleshooting control systems that use Allen-Bradley small logic controllers.

You should have a basic understanding of SLC 500™ products. You should understand programmable controllers and be able to interpret the ladder logic instructions required to control your application. If you do not, contact your local Rockwell Automation representative for information on available training courses before using this product.

Purpose of This Manual

As much as possible, we organized this manual to explain, in a task-by-task manner, how to install, configure, program, operate and troubleshoot an SLC 500-based system using the 1746-HSCE2 module.

Related Documentation

The table below provides a listing of publications that contain important information about SLC™ products.

For	Read this document	Document number
A reference manual containing status file data, instruction set, and troubleshooting information	SLC 500™ Instruction Set Reference Manual	1747-RM001
A description of how to install and use your Modular SLC 500 programmable controller	SLC 500™ Modular Hardware Style User Manual	1747-UM011
An overview of the SLC 500™ family of products	SLC 500 Systems Selection Guide	1747-SG001
In-depth information on grounding and wiring Allen-Bradley programmable controllers	Allen-Bradley Programmable Controller Grounding and Wiring Guidelines	1770-4.1
A description of important differences between solid-state programmable controller products and hard-wired electromechanical devices	Application Considerations for Solid-State Controls	SGI-1.1
An article on wire sizes and types for grounding electrical equipment	National Electrical Code	Published by the National Fire Protection Association of Boston, MA
A glossary of industrial automation terms and abbreviations	Allen-Bradley Industrial Automation Glossary	AG-7.1

If you would like a manual, you can:

- view and download a free electronic version from the internet at **www.rockwellautomation.com/literature**
- purchase a printed manual by contacting your local Allen-Bradley distributor or Rockwell Automation sales office

Conventions Used In This Manual

The following conventions are used throughout this manual:

- Bulleted lists (like this one) provide information, not procedural steps.
- Numbered lists provide sequential steps or hierarchical information.
- *Italic* type is used for emphasis.
- Text in this `font` indicates words or phrases you should type.

Your Questions or Comments on the Manual

If you find a problem with this manual, please notify us. If you have any suggestions for how this manual could be made more useful to you, please contact us at the address below:

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Module Overview

This chapter contains the following:

- multi-channel high-speed counter module overview
- operating class
- hardware features

Multi-Channel High-Speed Counter Module Overview

The 1746-HSCE2 is an intelligent counter module with its own microprocessor and I/O that is capable of reacting to high-speed input signals without the intervention of the SLC processor. The module is compatible with the SLC 500 family and can be used in a remote chassis with the SLC Remote I/O Adapter Module (1747-ASB).

Counters

The module is able to count in either direction. A maximum of four pulse counters are available (or 2 quadrature counters). Each counter can count to +/- 8,388,607 as a ring or linear counter. In addition to providing a count value, the module provides a rate value up to +/-1 MHz, dependent on the type of input. The rate value is the input frequency (in Hertz) to the counter. When the count value is increasing, the rate value is positive. When the count value is decreasing, the rate value is negative.

Counters can also be preset to any value between the minimum and maximum values. The conditions that preset the count value and generate capture values are configured by the gate/preset modes. The four counters can have different gate/preset modes.

Inputs

The module features six high-speed differential inputs labeled ±A1, ±B1, ±Z1, ±A2, ±B2, and ±Z2. It supports quadrature encoders with ABZ inputs and/or up to six discrete switches. In addition, x1, x2, and x4 counting configurations are provided to fully use the capabilities of high resolution quadrature encoders. The inputs can be wired for single-ended or differential use. Inputs are opto-isolated from the backplane.

Outputs

Eight outputs are available, four real (dc sourcing) and four virtual bits. The virtual outputs are available to the processor only. The real outputs are protected from overloads by a self-resetting fuse. The outputs can be controlled by any or all of the counters and/or directly controlled by the user's program.

Up to 16 dynamically configurable ranges are available, using rates or counts to control outputs. The ranges, programmed with range start and range stop values, can overlap. If the count or rate is within more than one range, the output patterns of those ranges are combined (logically ORed) to determine the actual status of the output. When an output is enabled by more than one counter and/or with the user program, its output state is determined by logically ORing the programmed setpoints of all those counters and the user program.

Operation

Module operation is controlled by user-programmed settings in the following six module programming blocks.

- Module Setup Block
- Counter Configuration Block
- Minimum/Maximum Count Value Block
- Minimum/Maximum Rate Value Block
- Program Ranges Block
- Counter Control Block

Most programming parameters, except those in the Module Setup and Counter Configuration blocks, are dynamic and can be changed without halting counter operation. The table below lists the static and dynamic parameters by programming block.

Programming Block	Parameter	Type[1]
Module Setup	Operating Mode	Static
	Range Allocation	
	Interrupt Enable	
	Rate Value Format	
Counter Configuration	Counter Type	Static[2]
	Input Configuration	
	Gate/Preset Mode	
Min./Max. Count Value	Minimum Count	Static[2]
	Maximum Count	Static[2]
	Preset Value	Dynamic[3]
Min./Max. Rate Value	Minimum Rate	Dynamic
	Maximum Rate	
Program Range	Counter Number	Dynamic
	Range Type	
	Range Number	
	Start Value	
	Stop Value	
	Output Image	
Counter Control	Enabled	Dynamic
	Soft Preset Only	
	Internal Direction	
	Output ON Mask	
	Output OFF Mask	
	Count or Rate Value	
	Range Enable Mask	

(1) STATIC = the associated counter must be disabled to set this parameter.
DYNAMIC = this parameter may be changed while the associated counter is running.

(2) Only the selected counter must be disabled.

(3) Under specific conditions, this parameter is dynamic. See page 4-15 for more information.

Operating Class

Module operation differs slightly based on the operating class. The operating class is selected via the module ID code.

Class 1

Class 1 operation is compatible with all SLC 500 processors. In Class 1 operation, the module uses 8 input and 8 output words and has an associated ID code of 3511. A maximum of four 16-bit counters are available in this operating class.

Class 4

Class 4 operation is compatible with SLC 5/03 and above systems. In Class 4 operation, the module uses 23 input and 8 output words and has an associated ID code of 15912. A maximum of four 24-bit counters are available in this class.

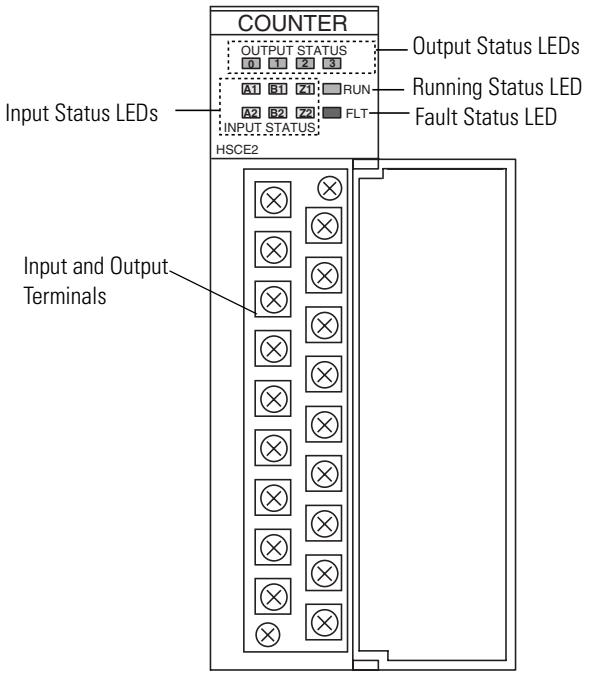
Class 1 vs. Class 4 Comparison

Class	Class 1	Class 4
Counters	16-bit (±32,767)	24-bit (±8,388,607)
Input Words	8 with limited information.	23 with all information.
Backplane Interrupts	Not permitted.	Permitted.
Use in RIO Chassis	Permitted.	Not permitted.
Use in ControlNet Chassis	Not permitted.	Permitted.
Module ID Code	3511	15912

Hardware Features

The module's hardware features are illustrated below. Refer to Chapter 3 for detailed information on installation and wiring.

Figure 1.1 Hardware Features



LEDs

The front panel has a total of twelve indicator LEDs, as shown in Figure 1.1 on page 1-5.

LED	Color	Indicates
0 OUT	Green	ON/OFF status of real output
1 OUT	Green	ON/OFF status of real output
2 OUT	Green	ON/OFF status of real output
3 OUT	Green	ON/OFF status of real output
RUN	Green	Running status of the module
FLT	Red	Steady on: Module fault Flashing: Output overcurrent
A1	Yellow	ON/OFF status of input A1
A2	Yellow	ON/OFF status of input A2
B1	Yellow	ON/OFF status of input B1
B2	Yellow	ON/OFF status of input B2
Z1	Yellow	ON/OFF status of input Z1
Z2	Yellow	ON/OFF status of input Z2

Jumpers

Six jumpers select the input voltages for the six inputs A1, B1, Z1, A2, B2, and Z2. The module accepts input voltages of 5V dc, 12V dc, or 24V dc. See Chapter 3 for jumper locations and settings.

Module Operation

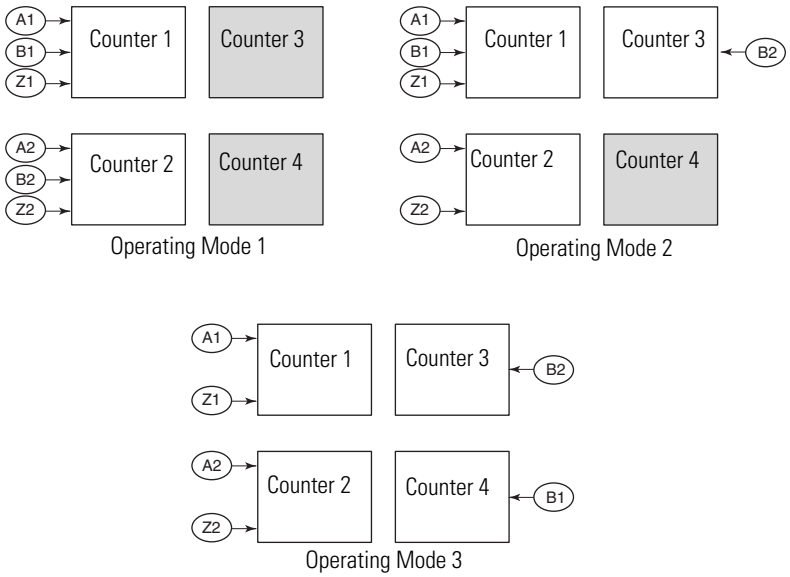
The chapter contains information about:

- operating modes
- input configurations
- gate/preset modes
- counter types
- rate value
- outputs
- range types

Operating Modes

The module's operating mode determines the number of available counters and which inputs are attached to them. The three operating modes and their input assignments are summarized in Figure 2.1.

Figure 2.1 Operating Mode Input Assignments



Input Configurations

Input configurations determine how the A and B inputs cause the counter to increment or decrement. The six available configurations are:

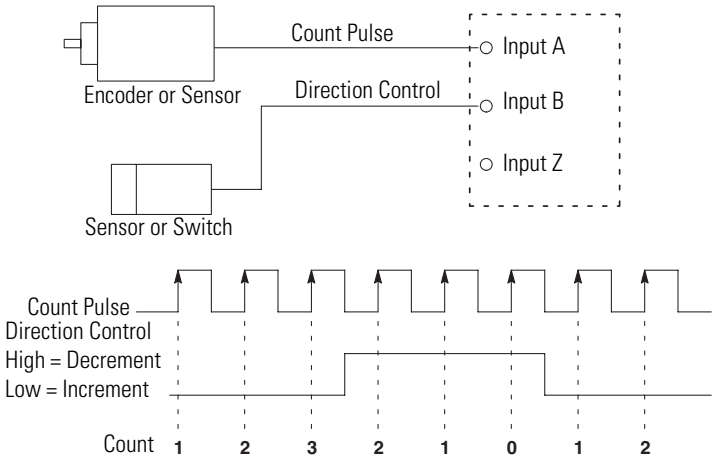
- Pulse/External Direction
- Pulse/Internal Direction
- Up and Down Pulses
- X1 Quadrature Encoder
- X2 Quadrature Encoder
- X4 Quadrature Encoder

See the Summary of Available Counter Configurations on page 2-8 for the input configurations available for the counters, based on operating mode.

Pulse/External Direction

With this configuration, the B input controls the direction of the counter, as shown below. If the B input is low (0), the counter increments on the rising edges of input A. If the input B is high (1), the counter decrements on the rising edges of input A.

Figure 2.2 Pulse/External Direction Configuration



Pulse/Internal Direction

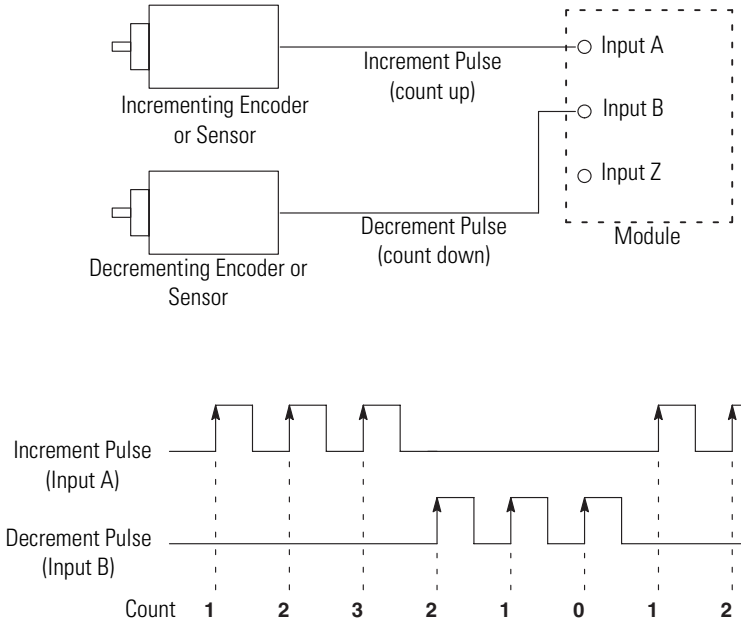
When the Pulse/Internal Direction configuration is selected, a bit written from the backplane determines the direction of the counter. The counter increments on the rising edge of the input if the bit is low (0) and decrements on the rising edge of the input if the bit is high (1).

Up and Down Pulses

In this configuration, the counter increments on the rising edge of pulses applied to input A and decrements on the rising edge of pulses applied to input B.

TIP When both inputs transition simultaneously or near simultaneously, the net result is no change to the count value. Therefore, simultaneous (or near simultaneous) pulses are ignored and no change in the count value is reported.

Figure 2.3 Up and Down Pulse Configuration



X1 Quadrature Encoder

When a quadrature encoder is attached to inputs A and B, the count direction is determined by the phase angle between inputs A and B. If A leads B, the counter increments. If B leads A, the counter decrements. The counter changes value *only* on one edge of input A as shown in Figure 2.4 on page 2-5.

TIP If B is low, the count increments on the rising edge of input A and decrements on the falling edge of input A. If B is high, all transitions on input A are ignored.

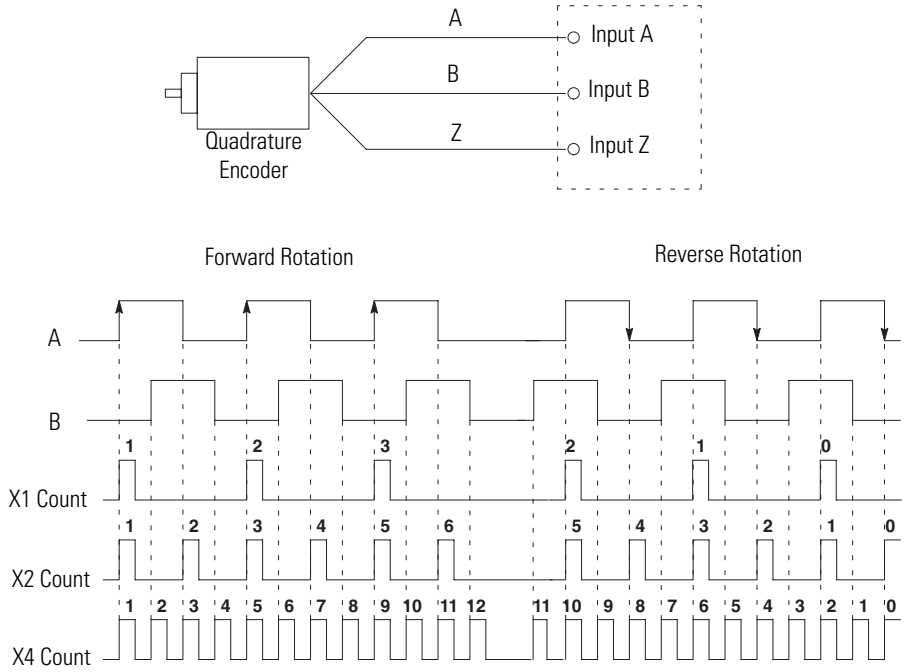
X2 Quadrature Encoder

Like the X1 Quadrature Encoder, the count direction is determined by the phase angle between inputs A and B. If A leads B, the counter increments. If B leads A, the counter decrements. However, the counter changes value on the *rising and falling* edges of input A, as shown in Figure 2.4 on page 2-5.

X4 Quadrature Encoder

Operation is similar to the X2 Quadrature Encoder configuration, except the counter changes value on the rising and falling edges of inputs A and B as shown in Figure 2.4.

Figure 2.4 Quadrature Encoder Configurations



IMPORTANT The input configuration is limited by the operating mode. In mode 1, Counters 1 and 2 can be assigned any input configuration. In mode 2, Counter 1 can be assigned any configuration, but Counters 2 and 3 are configured as pulse/internal direction. In mode 3, all counters have the pulse/internal direction configuration. See the Summary of Available Counter Configurations on page 2-8.

Input Frequency

Input frequency is determined by the input configuration as shown in the table below.

Input Configuration	Input Frequency
X4 Quadrature Encoder	250 kHz
X2 Quadrature Encoder	500 kHz
All Other Configurations	1 MHz

IMPORTANT The minimum high and low times for the pulse train are 475 ns. Therefore, the input pulse train must fall between a 47.5 to 52.5 percent duty cycle at 1 MHz.

Gate/Preset Modes

A counter's gate/preset mode determines what, if any, gating is applied to the counter and what, if any, conditions will preset the counter to the preset value. The Z inputs are the only inputs used for gating or presetting. The six gate/preset modes are described below.

No Preset

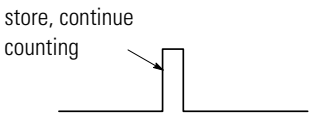
The counter is not preset under any conditions. The Z inputs are not used.

Soft Preset Only

The counter is preset when the matching preset bit in the SLC 500 output image table experiences a positive transition, but not in response to the Z input.

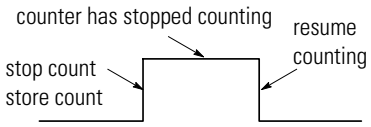
TIP The soft preset bit operates in all the gate/preset modes except No Preset.

Store/Continue



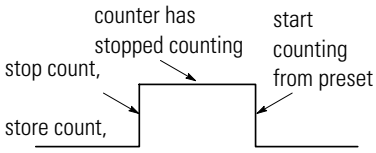
The count value is captured when the module detects an inactive-to-active transition on the Z input of the counter. This stored value is made available to the backplane. A stored status bit in the input image table is set to signal the processor that a new value is available. This bit is active until the capture value is read by the processor. Therefore, it is on for a maximum of 10 ms in Class 1, and a maximum of one scan or 10 ms, whichever is shorter, in Class 4. If a second capture event occurs before the first is read, the first value is lost. The count and rate values are not affected by a store event.

Store/Hold/Resume



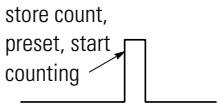
The count value, captured when the module detects a positive transition on the Z input, is made available to the backplane. A stored status bit is set in the input image table to signal the processor that a new value is available. This bit is active until the capture value is read by the processor. Therefore, it is on for a maximum of 10 ms in Class 1, and a maximum of one scan or 10 ms, whichever is shorter, in Class 4. The count value is held as long as the Z input is active. Because the count value is not changing, the rate value is equal to zero while the counter is held.

Store/Preset/Hold/Resume



The counter is set to its programmed preset value when the module detects a positive transition on the Z input of the counter. The capture value is made available to the backplane. A stored status bit is set in the input image table to signal the processor that a new value is available. This bit is active until the capture value is read by the processor. Therefore, it is on for a maximum of 10 ms in Class 1, and a maximum of one scan or 10 ms, whichever is shorter, in Class 4. The preset counter value is held as long as the Z input remains active. Because the count value is not changing, the rate value equals zero while the preset value is held.

Store/Preset/Start



The counter is set to its programmed preset value when the module detects a positive transition on the Z input of the counter. The capture value is made available to the backplane. A stored status bit is set in the input image table to signal the processor that a new value is available.This bit is active until the capture value is read by the processor. Therefore, it is on for a maximum of 10 ms in Class 1, and a maximum of one scan or 10 ms, whichever is shorter, in Class 4.

Gate and Preset Limitations

Because only the Z inputs are used for external gating and presetting, the only gate/preset modes available for Counters 3 and 4 are No Preset and Soft Preset Only. All six modes are always available for Counters 1 and 2.

IMPORTANT In Class 1, Operating Mode 2, Counter 2 does not have a capture value available. In Class 1, Operating Mode 3, no capture values are available.

Gate and Preset Considerations

Z-pulse Preset Operation

In applications where the Z pulse of the encoder is being used to preset the position, and where the Z pulse of the encoder is aligned with either the A or B pulses, the capture or count value may be affected by ± 1 count. If the Z pulse is edge aligned with the A pulse, preset operations may not be performed accurately in any of the quadrature modes. If the Z pulse is edge aligned with the B pulse, preset operation may not be performed accurately in the X4 quadrature mode only. A small capacitor (for example, 0.01 µF) across the Z inputs will dis-align these inputs and should correct this condition.

Summary of Available Counter Configurations

The table below summarizes the input configurations and gate/preset modes available for all counters, based on operating mode.

Operating Mode	Counter	Input Configuration	Gate/Preset Mode
1	1	All	All
	2	All	All
2	1	All	All
	2	Pulse/Internal Direction	All
	3	Pulse/Internal Direction	No Preset or Soft Preset Only
3	1	Pulse/Internal Direction	All
	2	Pulse/Internal Direction	All
	3	Pulse/Internal Direction	No Preset or Soft Preset Only
	4	Pulse/Internal Direction	No Preset or Soft Preset Only

Counter Types

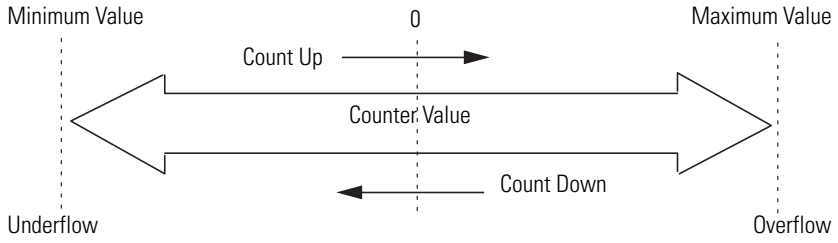
Each counter can be programmed to operate as a linear or ring counter. Both types are described below.

Linear Counter

The figure below demonstrates linear counter operation. In linear operation, the count value must remain within the programmed minimum/maximum values. If the count value goes above or below these values, the counter stops counting, and an overflow/underflow bit is set. In the overflow or underflow condition, the rate value continues to be updated and valid.

The number of pulses accumulated in an overflow/underflow state are ignored. The counter begins counting again when pulses are applied in the proper direction. For example, if you exceed the maximum by 1,000 counts, you do not need to apply 1,000 counts in the opposite direction before the counter begins counting down. The first pulse in the opposite direction decrements the counter.

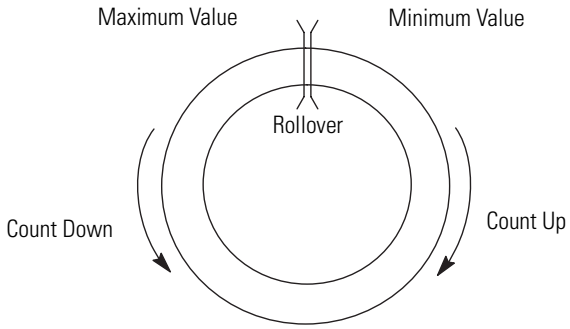
Figure 2.5 Linear Counter Diagram



Ring Counter

Figure 2.6 demonstrates ring counter operation. In ring counter operation, the count value changes between programmable minimum and maximum values. If, when counting up, the counter reaches the maximum value, it rolls over to the minimum value. If, when counting down, the counter reaches the minimum value, it rolls over to the maximum value.

Figure 2.6 Ring Counter Diagram



Rate Value

The rate value reported to the processor is calculated in counts per second (Hz), and is available with all input configurations. The input configuration determines how the rate value is calculated. When the count value is increasing, the rate value is positive. When the count value is decreasing, the rate value is negative.

The rate value is generally calculated as follows:

When the first input pulse is received, the value of an independent, free-running timer (Ta) is recorded. The module waits approximately 16 ms, while counting more input pulses. After 16 ms, the module waits for the next input pulse, and the value of the independent timer (Tb) is again recorded. The module then calculates the rate value using the formula:

$$\text{rate value} = \left(\frac{\text{number of counts}}{Tb - Ta}\right)$$

Additional checks ensure that rates below 1 Hz, which are not supported by the module, and frequencies due to motor vibration, are not counted in the rate value calculation.

Table 2.1 Typical Rate Update Times

Rates (Hz)	Time Between Pulses (ms)	Time Between Updates (ms)
1 to 59	17 to 1000	17 to 1000
60 to 1000	0 to 16	0 to 33
Above 1000	0 to 1	16

IMPORTANT

Because of the way the 1746-HSCE2 performs rate value calculations, invalid rate measurements may occur if the input frequency is below 60 Hz. Therefore, we recommend that the 1746-HSCE2 module not be used for rate monitoring or rate range control for frequencies below 60 Hz.

The invalid measurements apply only to rate values and do not affect the count value reported to the controller, which are always correct.

Accuracy

The accuracy of the rate value can be ±0.005% (typical). For this resolution, the rate measurement value must be transferred in single-precision floating-point format. This format is only available when the module operates as Class 4. Fractional rates, those between 1 and 0 or -1 and 0, are not reported.

The rate measurement value can also be transferred as an integer value. The integer format is available in both Class 1 and Class 4.

Output Control

All eight outputs can be controlled by any or all of the counters, or they can be controlled by the user program. When controlled by a counter, an output can be programmed to turn on or off based on the count value and/or rate value of the counter.

The eight outputs are divided into four real outputs and four virtual outputs. The outputs can be activated from the user program or from the module in response to specified input events. The status of the real outputs is available to the user program. The virtual outputs are available only to the user program. They have no real output associated with them. The real outputs are protected from overloads by a self-resetting fuse.

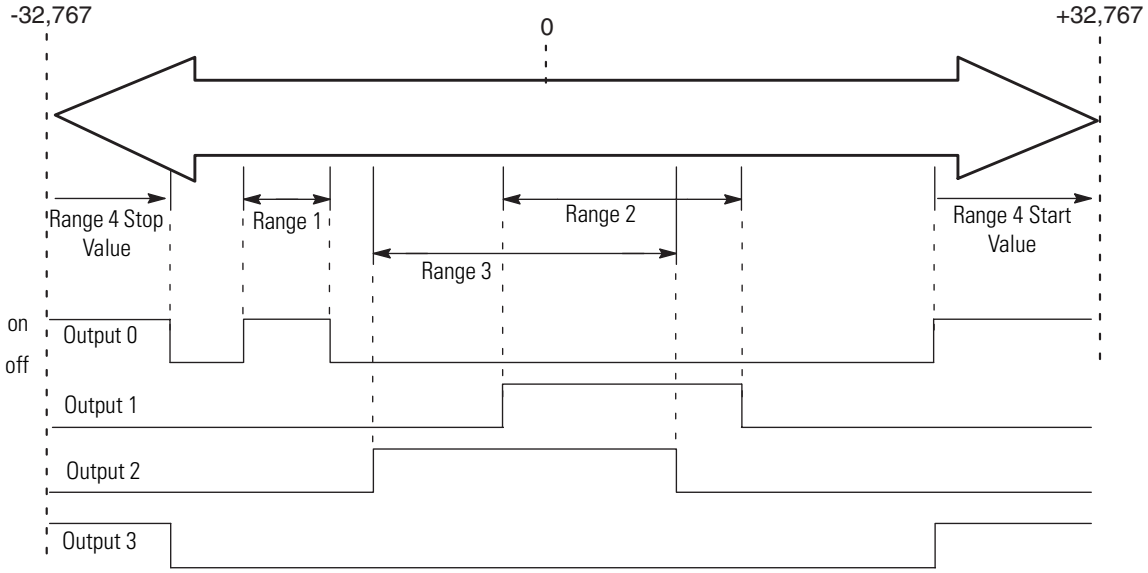
Range Control

The module can be programmed to use either counter or rate ranges to determine whether an output is active. Up to 16 dynamically configurable ranges are available. The ranges, programmed using range start and range stop values, can overlap. When the count is within more than one range, the output patterns of those ranges are combined (logically ORed) to determine the actual status of the output. A mixture of count ranges and rate ranges may be used.

Count Range

In a count range, the outputs are active if the count value is within the user-defined range. The valid count range is dependent upon the operating class. In Class 1, the valid range is -32,767 to +32,767. In Class 4, the valid range is -8,388,607 to +8,388,607. The examples in Figure 2.7 and Figure 2.8 use Class 1 operation.

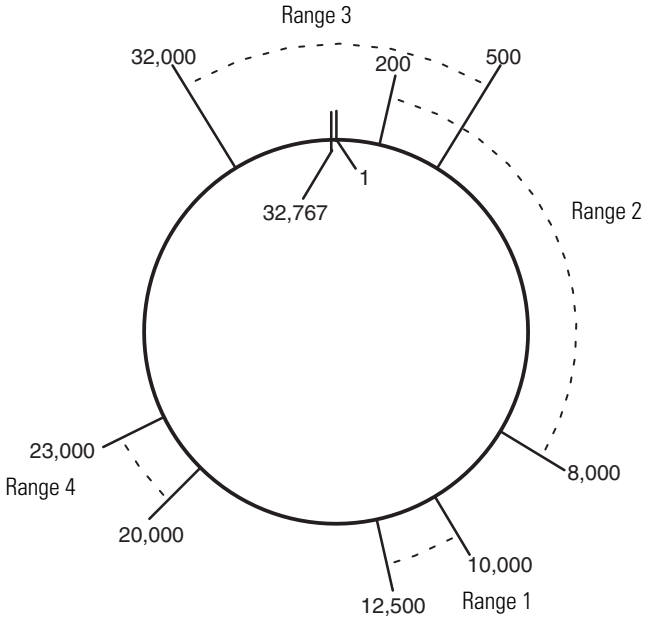
Figure 2.7 Count Range with Linear Counter



Range	Start Value	Stop Value	Outputs(1)								Outputs Affected
			7	6	5	4	3	2	1	0	
1	-7000	-5000	0	0	0	0	0	0	0	1	0
2	-1000	+4500	0	0	0	0	0	0	1	0	1
3	-4000	+3000	0	0	0	0	0	1	0	0	2
4	+9000	-9000	0	0	0	0	1	0	0	1	0 and 3

(1) Bits 0 through 3 are real outputs. Bits 4 through 7 are virtual outputs.

Figure 2.8 Count Range with Ring Counter



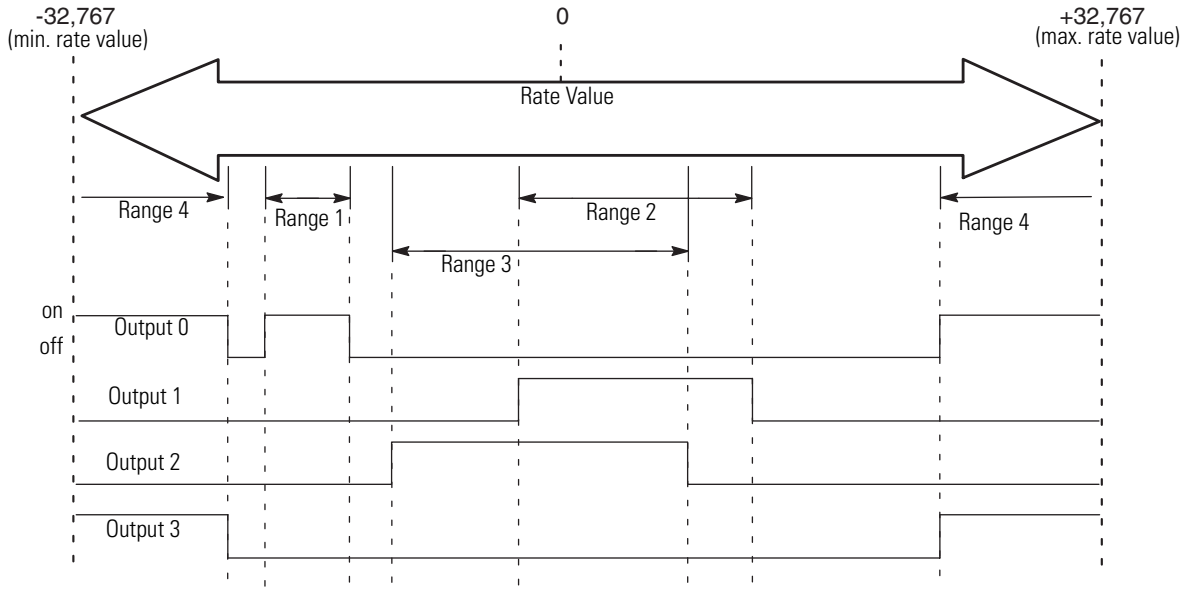
Range	Start Value	Stop Value	Outputs[1]								Outputs Affected
			7	6	5	4	3	2	1	0	
1	10,000	12,500	0	0	0	0	0	0	0	1	0
2	200	8,000	0	0	0	0	0	0	1	0	1
3	32,000	500	0	0	0	0	0	1	0	0	2
4	20,000	23,000	0	0	0	0	1	0	0	1	0 and 3

(1) Bits 0 through 3 are real outputs. Bits 4 through 7 are virtual outputs.

Rate Range

In a rate range, the outputs are active if the rate measurement is within the user-defined range. The valid input rate is dependent upon the operating class. In Class 1, the input rate can be up to 32,767 Hz in either direction. In Class 4, the input rate can be up to 1 MHz in either direction. The linear counter example in Figure 2.9 uses Class 1 operation.

Figure 2.9 Rate Range



Range	Start Value	Stop Value	Outputs[1]								Outputs Affected
			7	6	5	4	3	2	1	0	
1	-7000	-5000	0	0	0	0	0	0	0	1	0
2	-1000	+4500	0	0	0	0	0	0	1	0	1
3	-4000	+3000	0	0	0	0	0	1	0	0	2
4	+20000	-20000	0	0	0	0	1	0	0	1	0 and 3

(1) Bits 0 through 3 are real outputs. Bits 4 through 7 are virtual outputs.

Counter Input Data

The format of the counter input data table depends on the module's mode and class of operation. The status data formats for Class 1 and Class 4 are shown below, followed by explanations of the programming bits and status bytes. Mode 1 is the default for both Class 1 and Class 4 operation.

Class 1 Operation

In this operating class, the input data consists of eight words. The counters are sixteen bits. The data stored in an input word change based on the module's operating mode.

Figure 2.10 Mode 1 Input Data Format

	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
Word 0	ACK	MFLT	PERR	DEBUG	FB1	0	OP MODE		Output State							
									Virtual				Real			
Word 1	Counter 2 Status								Counter 1 Status							
Word 2	Counter 1: Count Value															
Word 3	Counter 1: Rate Value															
Word 4	Counter 1: Capture Value(1)															
Word 5	Counter 2: Count Value															
Word 6	Counter 2: Rate Value															
Word 7	Counter 2: Capture Value(1)															

(1) See page 2-6 for a description of capture values.

Figure 2.11 Mode 2 Input Data Format

	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
Word 0	ACK	MFLT	PERR	DEBUG	FB1	0	OP MODE		Output State							
									Virtual				Real			
Word 1	Counter 2: Status								Counter 1: Status							
Word 2	Counter 1: Count Value															
Word 3	Counter 1: Rate Value															
Word 4	Counter 1: Capture Value(1)															
Word 5	Counter 2: Count or Rate Value															
Word 6	0	0	0	0	0	0	0	0	Counter 3: Status							
Word 7	Counter 3: Count or Rate Value															

(1) See page 2-6 for a description of capture values.

Figure 2.12 Mode 3 Input Data Format

	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
Word 0	ACK	MFLT	PERR	DEBUG	FB1	0	OP MODE		Output State							
									Virtual				Real			
Word 1	Counter 2 Status								Counter 1 Status							
Word 2	Counter 1: Count or Rate Value															
Word 3	Counter 2: Count or Rate Value															
Word 4	Counter 4: Status								Counter 3: Status							
Word 5	Counter 3: Count or Rate Value															
Word 6	Counter 4: Count or Rate Value															
Word 7	Not Used. Set equal to 0000H															

Class 4 Operation

In Class 4 operation, the counter data consist of a maximum of 23 words.

Figure 2.13 Class 4 Data Format

	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00	
Word 0	ACK	MFLT	PERR	DEBUG	FB1	0	OP MODE		Output State								Transferred in all Modes[2]
									Virtual				Real				
Word 1	Counter 2 Status								Counter 1 Status								
Word 2	Upper 4 digits: Counter 1 Count Value																
Word 3	Lower 3 digits: Counter 1 Count Value																
Word 4	Counter 1 Rate Value[1]																
Word 5																	
Word 6	Upper 4 digits: Counter 1 Capture Value																
Word 7	Lower 3 digits: Counter 1 Capture Value																
Word 8	Upper 4 digits: Counter 2 Count Value																
Word 9	Lower 3 digits: Counter 2 Count Value																
Word 10	Counter 2 Rate Value[1]																
Word 11																	
Word 12	Upper 4 digits: Counter 2 Capture Value																
Word 13	Lower 3 digits: Counter 2 Capture Value																
Word 14	Counter 4 Status								Counter 3 Status								Transferred in Modes 2 and 3[2]
Word 15	Upper 4 digits: Counter 3 Count Value																
Word 16	Lower 3 digits: Counter 3 Count Value																
Word 17	Counter 3 Rate Value[1]																
Word 18																	
Word 19	Upper 4 digits: Counter 4 Count Value																Transferred in Mode 3[2]
Word 20	Lower 3 digits: Counter 4 Count Value																
Word 21	Counter 4 Rate Value[1]																
Word 22																	

(1) The format of the Rate Values is programmed with the Rate Value Format bit in the Module Setup programming block. This bit specifies the rate value to be in integer or floating-point format. The default is integer format. Count values are always transferred in integer format. See Data Format on page 4-3.

(2) Data values transferred. Regardless of operating mode, the module will transfer up to 23 words. Words that do not contain relevant data are set to 0000H.

Input Word Bit Values

ACK: Acknowledge Bit

This bit makes a 0 to 1 transition to signal the receipt of programming data.

MFLT: Module Fault Bit

This bit is set only if the module does not power up correctly. After a proper power up, the MFLT bit remains reset.

PERR: Programming Error Bit

The state of this bit is valid only when the acknowledge bit is set. This bit is reset when the last programming block is accepted without error. It is set when any one of the reserved bits are set or another programming error has occurred. For a list of other programming error conditions, see Module Programming Errors on page 5-3.

DEBUG: Debug Mode Bit

This bit is set when the debug mode is active.

IMPORTANT When the debug mode is active, the input data file shows the programming setup, not rate and count values.

For details, see Debug Mode Operation on page 5-7.

FB1: Fuse Status Bit

The FB1 fuse status bit is set (1) when the fuse is open. In addition, the module fault LED blinks to indicate an open fuse.

When FB1 is set (1), the real outputs do not function. Virtual outputs are not affected. The input word reflects this condition.

The module tries resetting the outputs at intervals of 500 ms. During each retry, the fuse status bit is reset (0). After the overload condition is corrected, the fuse bit resets (0) automatically.

OP MODE: Operating Mode Bits

The module uses these two bits to tell the processor what mode it is in. In class 1, the data value that an input word contains changes based on the operating mode.

Table 2.2 Mode Bit Settings

Bit 09	Bit 08	Mode
0	0	Reserved
0	1	Mode 1
1	0	Mode 2
1	1	Mode 3

Output State Byte

These bits correspond to the real or virtual state of the outputs. Bits 00 through 03 represent real outputs. Bits 04 through 07 represent virtual outputs.

Counter Status Bytes

Each counter has an associated status byte. The format of the byte depends on the module's class of operation as shown below.

Figure 2.14 Class 1 Counter Status Byte Format

15	14	13	12	11	10	09	08
07	**06**	**05**	**04**	**03**	**02**	**01**	**00**
C/R	0	ROvF	RUdF	COvF	CUdF	CState	

Figure 2.15 Class 4 Counter Status Byte Format

15	14	13	12	11	10	09	08
07	**06**	**05**	**04**	**03**	**02**	**01**	**00**
0	0	ROvF	RUdF	COvF	CUdF	CState	

C/R: Count/Rate Bit

The count/rate bit is used only in Class 1 operating mode. Because only one data word is available for Counters 2 and 3 in operating mode 2, and one data word for each of the four counters in operating mode 3, the module transfers either the counter's count or rate value.

When this bit is reset (0), the data in the corresponding word is the count value. When this bit is set (1), the data in the corresponding word is the rate value.

ROvF: Rate Overflow Bit

This bit is set when the rate is greater than the maximum rate value.

RUdF: Rate Underflow Bit

This bit is set when the rate is less than the minimum rate value.

COvF: Counter Overflow Bit

When the counter is configured as a linear counter, this bit is set when the count would become one over the maximum count value.

TIP Counter overflow or underflow bits are reset when a pulse in the opposite direction is received.

CUdF: Counter Underflow Bit

When the counter is configured as a linear counter, this bit is set when the count would become one under the minimum count value.

CState: Counter State Bits

These two bits show the operational state of the counter.

Table 2.3 Counter State Bit Settings

Bits 09 or 01	Bits 08 or 00	Operating State
0	0	Stopped
0	1	Running
1	0	Hold
1	1	Reserved

Installation and Wiring

This chapter provides the following information:

- compliance to European Union Directives
- module installation
- wiring considerations
- input/output connections
- encoder wiring
- switch wiring

Compliance to European Union Directives

If this product has the CE mark, it is approved for installation within the European Union and EEA regions. It has been designed and tested to meet the following directives.

EMC Directive

This product is tested to meet Council Directive 89/336/EED Electromagnetic Compatibility (EMC) and the following standards, in whole or in part, documented in a technical construction file:

EN50081-2
EMC — Generic Emission Standard, Part 2 – Industrial Environment

EN50082-2
EMC — Generic Emission Standard, Part 2 – Industrial Environment

This product is intended for use in an industrial environment.

Low Voltage Directive

This product is tested to meet Council Directive 73/23/EEC Low Voltage, by applying the safety requirements of EN 61131-2 Programmable Controllers, Part 2 – Equipment Requirements and Tests.

For specific information required by EN61131-2, see the appropriate sections in this publication, as well as the following Allen-Bradley publications:

- *Industrial Automation, Wiring and Grounding Guidelines for Noise Immunity*, publication 1770-4.1
- *Automation Systems Catalog*, publication B111

Prevent Electrostatic Discharge

ATTENTION

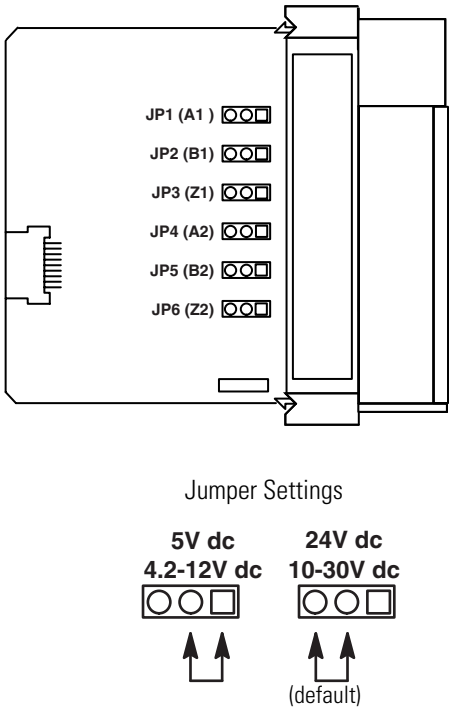
Static discharges may cause permanent damage to the module. Follow these guidelines when you handle the module:

- Touch a grounded object to discharge static potential.
- Wear an approved wrist-strap grounding device.
- Handle module by plastic case only. Avoid contact between module circuits and any surface which can hold an electrostatic charge.
- If available, use a static-safe work station.

Setting the Jumpers

Six jumpers are located in a column on the side of the module. Use the jumpers to select the input voltage for each of the inputs A1, B1, Z1, A2, B2, and Z2. The settings are shown in the figure on the following page.

Figure 3.1 Jumper Settings



IMPORTANT For a 12V dc encoder signal, use the 24V dc jumper setting.

ATTENTION If jumpers are not set to match the encoder type, the module may be damaged.

The 5V dc settings respond to inputs with an active voltage between 4.2 and 12 volts. The 24V dc settings respond to inputs with active or high settings between 10 and 30 volts.

Installing the Module

ATTENTION Disconnect power before attempting to install, remove, or wire the module.

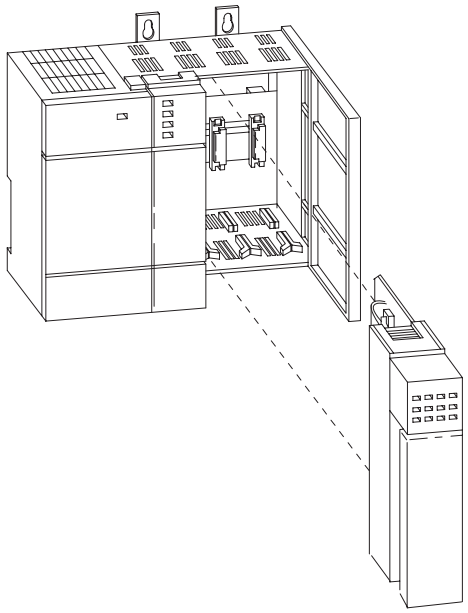
1. Make sure your SLC power supply has adequate reserve current capacity. The module requires 250 mA at +5V dc.

2. Align the full-sized circuit board with the chassis card guide as shown in Figure 3.2. The first slot of the first chassis is reserved for the processor.

3. Slide the module into the chassis until the top and bottom latches catch. To remove the module, press the release clips at the top and bottom of the module and slide it out.

4. Cover all unused card slots with the Card Slot Filler, catalog number 1746-N2.

Figure 3.2 Installing the Module



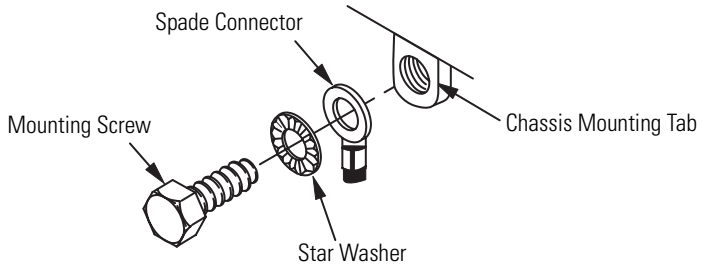
Important Wiring Considerations

Use the following guidelines when planning the system wiring for the module:

- Install the SLC500 system in a NEMA-rated enclosure.
- Disconnect power to the SLC processor and the module before wiring.
- Make sure the system is properly grounded.
- Group this module and low voltage DC modules away from AC I/O or high voltage DC modules.
- Shielded cable is required for high-speed input signals A, B, and Z. Use individually shielded, twisted-pair cable lengths up to 300 m (1000 ft.).

- Shields should be grounded only at one end. Ground the shield wire outside the module at the chassis mounting screw. Connect the shield at the encoder end only if the housing is electronically isolated from the motor and ground.

Figure 3.3 Grounding the Shield Wire at the Chassis Mounting Screw



- If you have a junction in the cable, treat the shields as conductors at all junctions. Do not ground them to the junction box.
- If your application requires only low frequency inputs, you can use a filter to minimize high frequency noise.
- If the Z pulse is edge aligned with A or B pulses, capture/preset operation may be affected by ± 1 count. A small capacitor (0.01µF) across the Z inputs will dis-align these inputs and should correct this condition. See Z-pulse Preset Operation on page 2-8.

Considerations for Reducing Noise

In high noise environments, the 1746-HSCE2 inputs may accept “false” pulses, particularly when using low frequency input signals with slowly sloping pulse edges. To minimize the effects of high frequency noise on low frequency signals, the user can do the following:

- Identify and remove noise sources.
- Route 1746-HSCE2 input cabling away from noise sources.
- Install low pass filters on input signals. Filter values are dependent on the application and can be determined empirically.
- Use devices which output differential signals, like differential encoders, to minimize the possibility that a noise source will cause a false input.

Electronic Protection

The electronic protection of the 1746-HSCE2 has been designed to provide protection for the module from overload current conditions. The protection is based on a thermal cut-out principle. In the event of a short circuit or overload current condition on an output channel, all channels will turn off within milliseconds after the thermal cut-out temperature has been reached.

IMPORTANT The module does not provide protection against reverse polarity wiring or wiring to AC power sources. Electronic protection is not intended to replace fuses, circuit breakers, or other code-required wiring protection devices.

Auto Reset Operation

IMPORTANT 1746-HSCE2 outputs perform auto-reset under overload conditions. When an output channel overload occurs as described above, all channels turn off within milliseconds after the thermal cut-out temperature has been reached. While the overcurrent condition is present, the module tries resetting the outputs at intervals of 500 ms. If the fuse cools below the thermal cut-out temperature, all outputs auto-reset and resume control of their external loads as directed by the module until the thermal cut-out temperature is again reached.

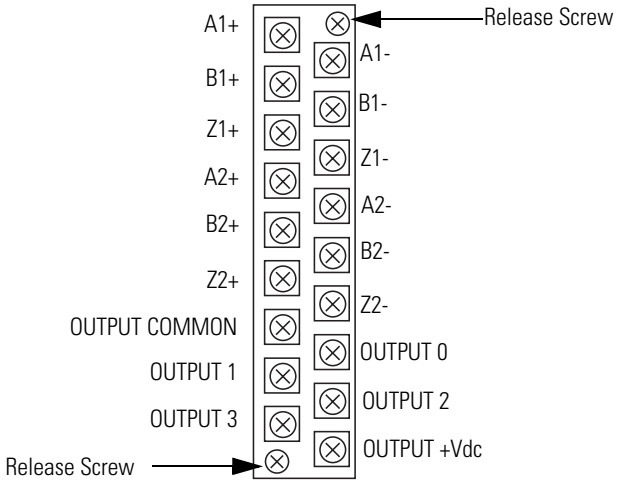
Removing power from an overloaded output channel would also allow the fuse to cool below the thermal cut-out temperature, allowing auto-reset to occur when power is restored. The output channels then operate as directed by the module until the thermal cut-out temperature is again reached.

To avoid auto-reset of output channels under overload conditions, monitor the fuse blown status bit (FB1) in the module's status file and latch the outputs off when an overcurrent condition occurs. An external mechanical fuse can also be used to open output circuits when they are overloaded.

Input and Output Connections

Input and output wiring terminals are shown in the figure below. Each terminal accepts #14 AWG wire. Tighten screws only tight enough to immobilize the wire. The torque applied to the screw should not exceed 0.9 Nm (8 in-lb.).

Figure 3.4 Terminal Wiring



Removing the Terminal Block

Remove the terminal block by turning the slotted terminal block release screws counterclockwise. The screws are attached to the terminal block, so it will follow as the screws are turned out.

ATTENTION

To avoid cracking the removable terminal block, alternate turning the slotted terminal block release screws.

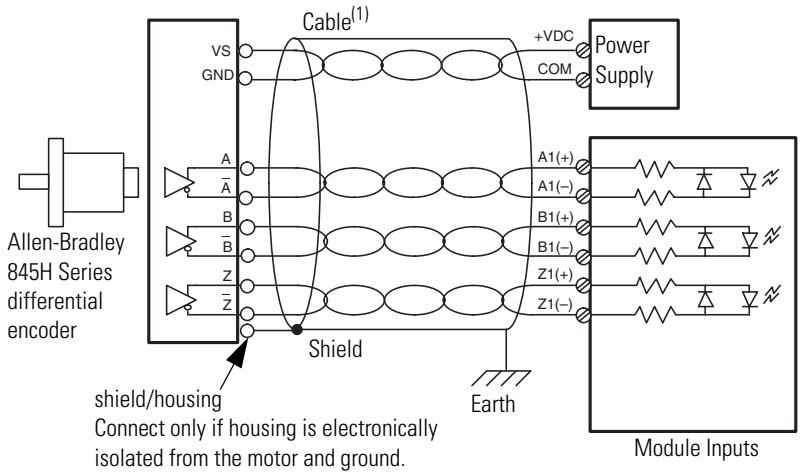
Encoder Wiring

Differential encoders provide the best immunity to electrical noise. We recommend, whenever possible, to use differential encoders.

The wiring diagrams on the following pages are provided to support the Allen-Bradley encoders you may already own.

Differential Encoder Wiring

Figure 3.5 Differential Encoder Wiring

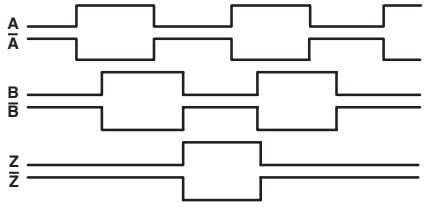


(1) Refer to your encoder manual for proper cable type. The type of cable used should be twisted pair, individually shielded cable with a maximum length of 300m (1000 ft.).

Differential Encoder Output Waveforms

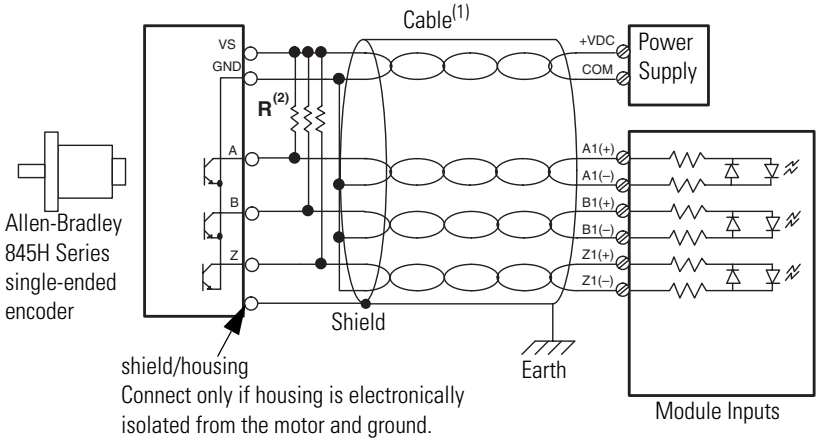
The Figure 3.6 shows the different encoder output waveforms. If your encoder matches these waveforms, the encoder signals can be directly connected to the associated screw terminals on the module. For example, the A lead from the encoder is connected to the module's A+ screw. If your encoder does not match these waveforms, some wiring modifications may be necessary. See Appendix B for a description of these modifications.

Figure 3.6 Differential Encoder Output Waveforms



Single-Ended Encoder Wiring (Open Collector)

Figure 3.7 Single-Ended Encoder Wiring



(1) Refer to your encoder manual for proper cable type. The type of cable used should be twisted-pair, individually shielded cable with a maximum length of 300m (1000 ft.).

(2) Calculate the value of the pull-up resistor (R), as shown below:

For 5V dc jumper position: $R = \frac{(Vcc - Vmin)}{Imin}$

For 24V dc jumper position: $R = \left(\frac{(Vcc - Vmin)}{Imin} - 1K\Omega\right)$

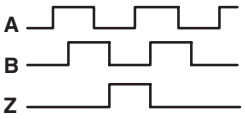
where:R = pull-up resistor value
Vcc = power supply voltage
Vmin = 4.2 V dc
Imin = 6.3 mA

Power Supply Voltage (Vcc)	Pull-up Resistor Value (R)
5V dc	127 Ω
12V dc	238 Ω
24V dc	2140 Ω

Single-Ended Encoder Output Waveforms

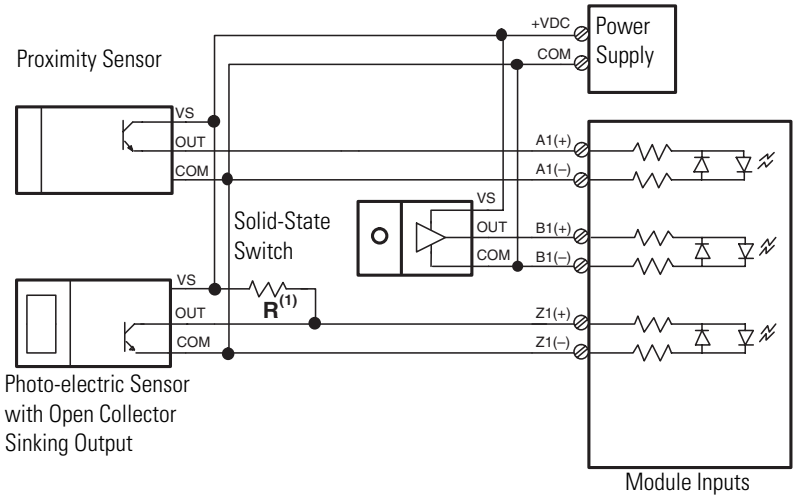
The figure below shows the single-ended encoder output waveforms. When the waveform is low, the encoder output transistor is on. When the waveform is high, the encoder output transistor is off.

Figure 3.8 Single-Ended Encoder Output Waveforms



Single-Ended Wiring (Discrete Devices)

Figure 3.9 Discrete Device Wiring



(1) Calculate the value of the pull-up resistor (R), as shown below:

For 5V dc jumper position: $R = \frac{(Vcc - Vmin)}{Imin}$

For 24V dc jumper position: $R = \left(\frac{(Vcc - Vmin)}{Imin} - 1\,K\Omega\right)$

where:R = pull-up resistor value
Vcc = power supply voltage
Vmin = 4.2 V dc
Imin = 6.3 mA

Power Supply Voltage (Vcc)	Pull-up Resistor Value (R)
5V dc	127 Ω
12V dc	238 Ω
24V dc	2140 Ω

Configuration and Programming

This chapter provides information about:

- selecting operating class
- module programming
- programming blocks
- programming block default values

Selecting Operating Class

The 1746-HSCE2 module has two operating classes which are determined by the ID code used by the module.

Class 1 operation uses 8 input and 8 output words and is compatible with SLC 5/01 and above processors and the 1747-ASB module. Enter ID Code 3511 to select Class 1 operation.

Class 4 operation uses 23 input and 8 output words and is compatible with SLC 5/03 and above processors and with 1747-ACN15 and -ACNR15 modules. Enter ID Code 15912 to select Class 4 operation.

See Operating Class on page 1-4 for more information on Class 1 and Class 4 operation.

Power-up Reset

Whenever power is cycled or the processor mode is switched to RUN, all counters are reset to their defaults. The counters, ranges, presets, etc., need to be reprogrammed. See the default settings on page 4-28.

Module Programming

Module programming consists of the following six blocks:

- Module Setup
- Counter Configuration
- Minimum/Maximum Count Value
- Minimum/Maximum Rate Value
- Program Ranges
- Counter Control

Each block is made up of eight words. The first word is the control word. The remaining seven words are data words. The control word determines which parameters are in the data words. This programming method applies to both classes of operation. The programming blocks are described on pages 4-6 through 4-23.

Programming Cycle

Except for the Counter Control Block, all programming blocks are written to the module with a programming cycle. Programming cycles are controlled by the transmit and acknowledge bits.

A programming cycle consists of six steps.

1. Write the new data into the correct output image table words. The lower byte of each configuration block indicates which block is being transferred. See the programming block descriptions on pages 4-6 to 4-28.

2. Each block that can be altered has a Transmit bit (O:e.0/15). Set the Transmit bit in the output image table. The 1746-HSCE2 will not act on the new programming block until the Transmit bit is set.

3. Once the Transmit bit is set, an Acknowledge bit (I:e.0/15) is received.

4. When the ladder logic detects that the Acknowledge bit is set, it should check for errors. Error bits are only valid when the Acknowledge bit is set. The error bits are the PERR bit (I:e.0/13) and the MFLT bit (I:e.0/14).

5. If either bit is set, the programming block is rejected. The block pointer is not incremented and initialization fails.

   If neither error bit is set, the block pointer is incremented and the Transmit bit is reset, allowing the module to transfer the next block.

6. Once the desired configurable blocks have been transferred to the module and the Maximum Block Address is recognized, the Counter Control Block is transferred to the output image table to enable the counters.

Data Format

In Class 4, the counter accepts rate data in either integer or floating-point data formats, depending upon the setting of the rate value bit. Both formats are explained below.

TIP Count values are always in integer format. The format of rate values is selected in the Module Setup Block as either integer or floating-point formats. All other data is in integer format.

Integer Format

In integer format, two words may be needed to hold each data value because the values can exceed ±32768 (decimal) when the module is in Class 4 operation. The combined decimal value of both words is calculated as follows:

actual value = (value of first word x 1000) + value of second word

Both word values must have the same sign or a programming error results. If the value is positive, both words must be positive. If the value is negative, both words must be negative.

TIP A value of zero in either word may be paired with either sign in the other word.

The following example illustrates how numbers are represented in integer format.

Table 4.1 Integer Format Example

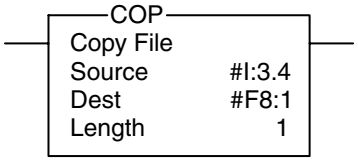
First Word	Second Word	Data
12	345	12,345
-12	-345	-12,345
12	0	12,000
-12	0	-12,000

Floating-Point Format

Floating-point notation (IEEE 754 single-precision used) is difficult to read and use, but may be simplified by using programming software to view and use the data in a floating-point file.

Reading the Data

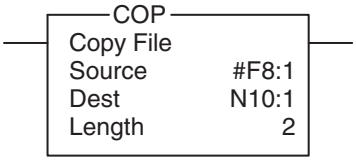
In the following example, the 1746-HSCE2 module is located in slot 3. The rate value, in floating point rate value format, is located in input data file words 4 and 5 (I:3.4 and I:3.5). To view the rate value for counter 1, use the copy instruction as shown below.



The source is the input data file, and the destination is the floating point file. The length is 1, the number of elements of the destination file in the COP instruction.

Writing the Data

In the following example the floating point value is copied into integer words 1 and 2 of the Minimum/Maximum Rate Value programming block (N10:0-7). The 1746-HSCE2 module is located in slot 3.

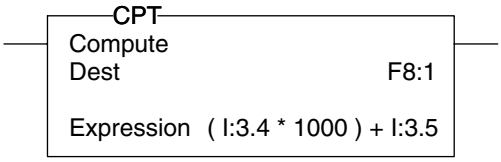


The source is the floating-point file, and the destination is an integer data file. The length is 2, the number of elements being copied into the destination file using the copy instruction.

Converting from Two-Word Integer to Floating-Point Format

You can use RSLogix500™ programming software to convert the values from integer to floating-point notation using the compute instruction, as shown.

In this example, the 1746-HSCE2 module is located in slot 3, the upper 4 digits of the rate value are stored in the input data file word 4 (I:3.4), and the lower 3 digits of the rate value are stored in input data file word 5 (I:3.5). The compute instruction is as follows:

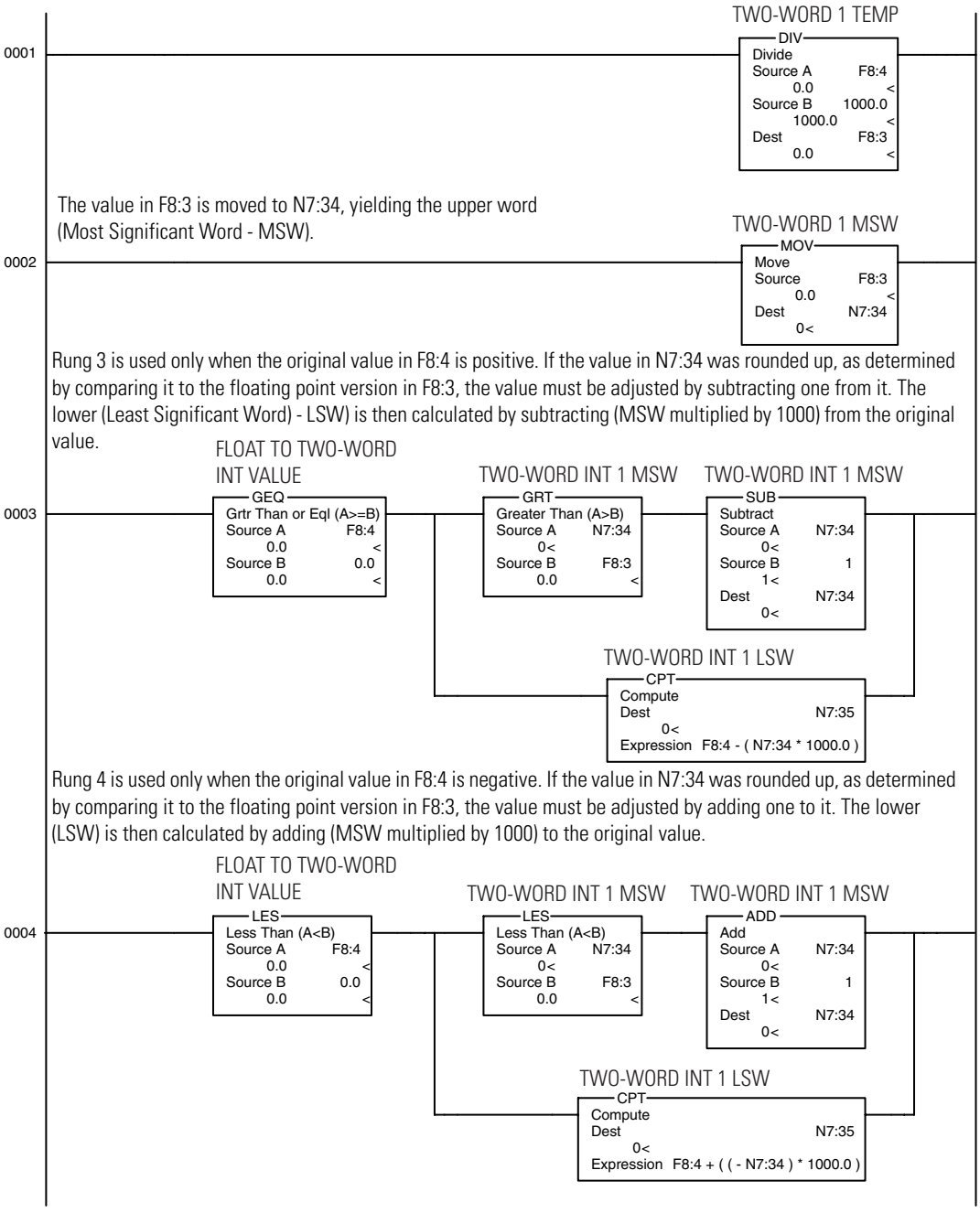


The destination is in the floating-point file F8.

Converting from Floating-Point to Two-word Integer Format

RSLogix500 programming software can also be used to convert from floating-point to two-word integer format as shown.

F8:4 holds the number to be converted. It is divided by 1000 and the result is placed in F8:3.



Module Setup Block

Figure 4.1 shows the format of the Module Setup block. This block sets the module's basic configuration and range allocation to the counters. Counters cannot be running when this block is sent to the module or a programming error results. Sending this block to the module sets all other module parameters to their default values. See Programming Block Default Values on page 4-28.

Figure 4.1 Module Setup Block Format

	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
Word 0	TRMT	0	0	DEBUG	0	0	0	0	0	0	0	0	0	0	0	1
Word 1	0	0	0	0	0	INT	RVF	PRA	0	0	0	0	0	0	Op Mode	
Word 2	0	0	0	0	0	0	0	0	0	0	0	Counter 1 Range Allocation				
Word 3	0	0	0	0	0	0	0	0	0	0	0	Counter 2 Range Allocation				
Word 4	0	0	0	0	0	0	0	0	0	0	0	Counter 3 Range Allocation				
Words 5-7	RESERVED: Must equal 0															

Programming Block Identification Bit (Word 0, Bit 0)

This bit identifies the type of block.

TRMT: Transmit Bit (Word 0, Bit 15)

A 0 to 1 transition starts a programming cycle. This bit is not set until all words are in the output table.

DEBUG: Debug Mode Selection Bit (Word 0, Bit 12)

When this bit is set, the debug mode is activated. Debug mode returns the input data file showing current settings in the module setup block.

Up to three sets of ranges can be allocated. The last set is always allocated automatically. If three sets of ranges are allocated, the fourth and last set is shown in word 5 in debug mode. For details, see Debug Mode Operation on page 5-7.

INT: Interrupt Enable
(Word 1, Bit 10)

IMPORTANT Interrupt mode is not available in Class 1. Setting this bit while using Class 1 causes a programming error.

In Class 4, when this bit is set (1), the module generates an I/O interrupt to the SLC processor whenever one of the eight outputs changes state. When this bit is reset (0), the module will not generate an interrupt.

IMPORTANT An I/O interrupt must be defined if the INT bit is set. The I/O interrupt subroutine number is defined in the advanced configuration window of the program's I/O configuration. See the *SLC 500 Instruction Set Reference Manual*, publication number 1747-RM001, for more information on I/O interrupts.

RVF: Rate Value Format
(Word 1, Bit 09)

IMPORTANT This bit is not used in Class 1. Setting this bit while using Class 1 causes a programming error.

In Class 4, the module transmits the rate value in a two-word integer format when this bit is reset (0). The module transmits the rate value in single-precision floating-point format when this bit is set (1).

PRA: Program Range Allocation
(Word 1, Bit 08)

When this bit is set (1), the module programs the range allocation to the values in words 2, 3, and 4.

Op Mode: Operating Mode
(Word 1, Bits 01 and 00)

These two bits program the module's operating mode. The combinations are shown below:

Table 4.2 Operating Mode Programming Bit Settings

Bit 01	Bit 00	Operating Mode
0	0	Reserved(1)
0	1	Mode 1
1	0	Mode 2
1	1	Mode 3

(1) Using the reserved setting causes a programming error.

Range Allocation Values
(Words 2, 3, and 4, Bits 00 to 04)

Sixteen ranges are available for programming output on/off positions and rates. These ranges are assigned to the counters using these range allocation parameters. Each value is the number of ranges assigned to each counter.

The operating mode parameter is read before the range allocation values. The module's operating mode determines which counters' allocation values are read.

- In Mode 1, two counters are used. Only the Counter 1 allocation value is read. All other ranges are automatically assigned to Counter 2. Set words 3 and 4 to 0.
- In Mode 2, three counters are used. The Counter 1 and Counter 2 allocation values are read. All other ranges are automatically assigned to Counter 3. Set word 4 to 0.
- In Mode 3, all four counters are used. The Counter 1, Counter 2, and Counter 3 allocation values are read. All other ranges are automatically assigned to Counter 4.

The sum of the range allocation values cannot exceed 16, or the module responds with a programming error. Unused range allocation words in Modes 1 and 2 must equal zero, or an error occurs.

IMPORTANT The number of ranges for the last configured counter used must equal zero, otherwise the module fills in the value and errors, even if the value is correct.

Range Allocation Examples

Mode 1 Example

In the Module Setup block below, 4 ranges are assigned to Counter 1. The remaining 12 are assigned to Counter 2. The last counter is not specified.

Figure 4.2 Module Setup in Mode 1 (Showing Hex Format)

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00		Hex			
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	**Word 0**	0	0	0	1
0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	1	**Word 1**	0	1	0	1
0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	**Word 2**	0	0	0	4
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	**Word 3**	0	0	0	0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	**Word 4**	0	0	0	0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	**Word 5**	0	0	0	0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	**Word 6**	0	0	0	0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	**Word 7**	0	0	0	0

Mode 2 Example

In the Module Setup block below, four ranges are assigned to Counter 1. Four ranges are assigned to Counter 2, with the remaining 8 assigned to Counter 3.

Figure 4.3 Module Setup in Mode 2 (Showing Hex Format)

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00		Hex			
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	**Word 0**	0	0	0	1
0	0	0	0	0	0	0	1	0	0	0	0	0	0	1	0	**Word 1**	0	1	0	1
0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	**Word 2**	0	0	0	4
0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	**Word 3**	0	0	0	4
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	**Word 4**	0	0	0	0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	**Word 5**	0	0	0	0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	**Word 6**	0	0	0	0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	**Word 7**	0	0	0	0

IMPORTANT The number of ranges for the last configured counter used must equal zero, otherwise the module fills in the value and errors, even if the value is correct.

Mode 3 Example

In the Module Setup block below, four ranges are assigned to Counter 1. Eight ranges are assigned to Counter 2. Two ranges are assigned to Counter 3. The last two ranges are assigned to Counter 4, but the counter is not specified.

IMPORTANT The number of ranges for the last configured counter used must equal zero, otherwise the module fills in the value and errors, even if the value is correct.

Figure 4.4 Module Setup in Mode 3 (Showing Hex Format)

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00		Hex			
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	**Word 0**	0	0	0	1
0	0	0	0	0	0	0	1	0	0	0	0	0	0	1	1	**Word 1**	0	1	0	3
0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	**Word 2**	0	0	0	4
0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	**Word 3**	0	0	0	8
0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	**Word 4**	0	0	0	2
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	**Word 5**	0	0	0	0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	**Word 6**	0	0	0	0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	**Word 7**	0	0	0	0

Counter Configuration Block

Figure 4.5 shows the format of the Counter Configuration Block. This block programs the following parameters of the selected counters:

- Counter Type
- Input Configuration
- Gate/Preset Mode

All four counters can be programmed with one block. When this programming block is sent to the module, the selected counter(s) cannot be running or a programming error results. Sending this programming block to the module erases all programmed output ranges of the selected counter(s).

Figure 4.5 Counter Configuration Block Format

	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00	
Word 0	TRMT	0	0	DEBUG	PGM4	PGM3	PGM2	PGM1	0	0	0	0	0	0	1	0	
Word 1	0	0	0	0	0	0	0	0	0	G/P Mode			Input Config			CType	Counter 1
Word 2	RESERVED: Must equal 0																
Word 3	0	0	0	0	0	0	0	0	0	G/P Mode			Input Config			CType	Counter 2
Word 4	RESERVED: Must equal 0																
Word 5	0	0	0	0	0	0	G/Pmode	CType	0	0	0	0	0	0	G/Pmode	CType	Counter 3 or 4 as indicated
	Counter 4								Counter 3								
Word 6	RESERVED: Must equal 0																
Word 7	RESERVED: Must equal 0																

Programming Block Identification Bit (Word 0, Bit 01)

This bit identifies the type of block.

TRMT: Transmit Bit (Word 0, Bit 15)

A 0 to 1 transition starts a programming cycle.

DEBUG: Debug Mode Selection Bit (Word 0, Bit 12)

When this bit is set, the debug mode is activated. Debug mode returns the input data file showing current settings in the counter configuration block. See Debug Mode Operation on page 5-7.

PGM*n*: Program Counter Number Bits
(Word 0, Bits 08 to 11)

These four bits select the counters to which the programming block is applied. If the bit is reset, the associated counter is not programmed and the counter can be running when this block is sent. In addition, the associated programming words must be zero or a programming error occurs. A counter must be stopped when programmed with this block.

CType: Counter Type Bit
(Words 1 and 3, Bit 00; Word 5, Bits 00 and 08)

For each counter, this bit defines whether the counter is a ring or linear counter.

Table 4.3 Counter Type Programming Bit Settings

Bit	Counter Type
0	Ring Counter
1	Linear Counter

Input Config: Input Configuration Bits
(Words 1 and 3, Bits 01 to 03)

These bits define the input configuration for Counters 1 and 2. Counters 3 and 4 are always Pulse/Internal Direction counters and do not require programming bits. The table below shows the input configuration programming bit values.

Table 4.4 Input Configuration Programming Bit Settings

Bit 03	Bit 02	Bit 01	Input Configuration
0	0	0	RESERVED
0	0	1	Up/Down Pulses
0	1	0	Pulse/External Direction
0	1	1	Pulse/Internal Direction
1	0	0	Quadrature X1
1	0	1	Quadrature X2
1	1	0	Quadrature X4
1	1	1	RESERVED

G/P Mode: Gate/Preset Mode Bits
(Words 1 and 3, Bits 04 to 06; Word 5, Bits 09 and 01)

Counters 3 and 4 have only two gate/preset modes available. Therefore, they have only one G/P mode bit. When this single bit is equal to zero, the No Preset mode is selected. When the bit is set, the Soft Preset mode is selected. Three bits determine the Gate/Preset Mode for Counters 1 and 2. The table below shows the G/P Mode settings for counters 1 and 2.

Table 4.5 Gate/Preset Mode Programming Bit Settings for Counters 1 and 2

Bit 06	Bit 05	Bit 04	Gate/Preset Mode
0	0	0	No Preset
0	0	1	Soft Preset Only
0	1	0	RESERVED
0	1	1	RESERVED
1	0	0	Store/Continue/Soft Preset
1	0	1	Store/Hold/Resume/Soft Preset
1	1	0	Store/Preset/Hold/Resume/Soft Preset
1	1	1	Store/Preset/Start/Soft Preset

TIP All configurations and modes are not available to all counters. See the Summary of Available Counter Configurations on page 2-8.

Minimum/Maximum Count Value Block

Figure 4.6 shows the format of the Minimum/Maximum Count Value block. This programming block programs the minimum and maximum counter value and preset value parameters of the selected counter. As long as the min/max counter values are not changed from their currently programmed values, the counter can be running when this block is sent to the module. If the minimum/maximum values are changed, the counter must be stopped when this block is sent or a programming error is generated. The preset values can be changed with the counter running.

Figure 4.6 Minimum/Maximum Count Value Block

	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
Word 0	TRMT	0	0	DEBUG	0	AUTO PRESET	CNTR No		0	0	0	0	0	1	0	0
Word 1	Upper 4 digits: Minimum Count Value															
Word 2	Lower 3 digits: Minimum Count Value															
Word 3	Upper 4 digits: Maximum Count Value															
Word 4	Lower 3 digits: Maximum Count Value															
Word 5	Upper 4 digits: Preset Value															
Word 6	Lower 3 digits: Preset Value															
Word 7	RESERVED: Must equal zero															

Programming Block Identification Bit (Word 0, Bit 02)

This bit identifies the type of block.

TRMT: Transmit Bit (Word 0, Bit 15)

A 0 to 1 transition starts a programming cycle.

DEBUG: Debug Mode Selection Bit (Word 0, bit 12)

When this bit is set, the debug mode is activated. Debug mode returns the input data file showing current settings in the Min./Max. Count Value block. For details, see Debug Mode Operation on page 5-7.

AUTO PRESET: Automatic Preset Bit (Word 0, bit 10)

This bit is used to automatically preset the count value. If this bit is set (1) when the programming block is sent, the count value is set to its preset value. If the bit is reset (0), the count value is not changed.

CNTR No.: Counter Number Bits
(Word 0, Bit 08 and 09)

These two bits select the counter to which this programming block is applied.

Table 4.6 Counter Number Bit Settings

Bit 09	Bit 08	Counter Number
0	0	Counter 1
0	1	Counter 2
1	0	Counter 3
1	1	Counter 4

Preset Value
(Words 5 and 6)

The preset value can be programmed to any number between the minimum count value and the maximum count value. If the preset value does not fall between the minimum and maximum count values, a programming error results. The preset value is specified in the two-word integer data format as described in Integer Format on page 4-3. This value may be changed with the counter running, if minimum and maximum values are equal to their previously programmed values.

Minimum/Maximum Count Value Words
(Words 1 to 4)

The valid range of the parameter is dependent upon the operating class.

Table 4.7 Minimum/Maximum Count Values by Class

Class 1 Count Value		Class 4 Count Value	
Minimum	-32,767 to +32,766	Minimum	-8,388,607 to +8,388,606
Maximum	(Min. Value +1) to +32,767	Maximum	(Min. Value +1) to +8,388,607

The minimum/maximum count value can be changed after the output ranges have been programmed. However, they cannot be changed while the counter is enabled. When the minimum/maximum values are changed, they are checked against the ranges. If any of the new values are outside the range boundaries, the new values are not accepted, and the programming error bit is set. The preset value is

always included with this block, and its value must fall between the minimum/maximum count values.

The data is in the two-word integer format as described in Integer Format on page 4-3.

Counter Type

The meanings of the minimum and maximum counter values are dependent on the counter type.

Ring Counter

As a ring counter, the counter counts between the minimum and maximum values. When counting up, if the maximum value is reached, the counter rolls over to the minimum value. When counting down, if the minimum value is reached, the counter rolls over to the maximum value.

Linear Counter

As a linear counter, the counter counts between the minimum and the maximum value. If the maximum value would be exceeded when the counter is counting up, the counter stops counting and an overflow bit is set in the status field of the counter. If, while counting down, the counter reaches a value that would be less than the minimum value, an underflow bit is set in the status field of the counter.

The number of pulses accumulated in an overflow/underflow state are ignored. The counter begins counting again when pulses are applied in the proper direction. For example, if you exceed the maximum by 1,000 counts, you do not need to apply 1,000 counts in the opposite direction before the counter begins counting down. The first pulse in the opposite direction decrements the counter.

If the linear counter is in an overflow/underflow state, the rate value continues to update.

Minimum/Maximum Rate Value Block

Figure 4.7 shows the format of the Minimum/Maximum Rate Value programming block. This block programs the minimum and maximum rate values of the selected counter. All counters can be running when this block is sent to the module.

Figure 4.7 Min./Max. Rate Value Block

	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
Word 0	TRMT	0	0	DEBUG	0		CNTR No.		0	0	0	0	1	0	0	0
Word 1	Minimum Rate Value in integer or floating point notation															
Word 2																
Word 3	Maximum Rate Value in integer or floating point notation															
Word 4																
Word 5-7	RESERVED: Must equal zero															

Programming Block Identification Bit (Word 0, Bit 03)

This bit identifies the type of block.

TRMT: Transmit Bit (Word 0, Bit 15)

A 0 to 1 transition starts a programming cycle.

DEBUG: Debug Mode Selection Bit (Word 0, bit 12)

When this bit is set, the debug mode is activated. Debug mode returns the input data file showing current settings in the Min./Max. Rate Value block. For details, see Debug Mode Operation on page 5-7.

CNTR No.: Counter Number Bits (Word 1, Bits 08 and 09)

These two bits select the counter to which this programming block is applied.

Table 4.8 Counter Number Bit Settings

Bit 09	Bit 08	Counter Number
0	0	Counter 1
0	1	Counter 2
1	0	Counter 3
1	1	Counter 4

Minimum/Maximum Rate Value Words (Words 1 to 4)

The valid range of this parameter is dependent on the operating class of the module.

Class 1 Rate Value (Hz)		Class 4 Rate Value (Hz)	
Minimum	-32,767 to +32,766	Minimum	-1,000,000 to +999,999
Maximum	(Min. Value +1) to +32,767	Maximum	(Min. Value +1) to +1,000,000

If the calculated rate value is less than the minimum value, a rate underflow bit is set in the input image table. If the calculated rate value is greater than the maximum value, a rate overflow bit is set in the input image table. Outputs assigned to the counter still function normally.

Operating Class

The format of the minimum/maximum rate values depends on the operating class of the module.

Class 1

When the module is operating as Class 1, the minimum/maximum rate values are programmed in two-word integer format.

Class 4

When the module is operating as Class 4, the data format of the minimum/maximum rate values is determined by the rate value format bit in the Module Setup programming block. When this bit specifies that the rate value be in floating-point format, the minimum/maximum rate values are also programmed in floating-point format. When the rate value format bit specifies integer format, the minimum/maximum rate value is also in two-word integer format.

When programmed in integer format, the data has the same format as described in Integer Format on page 4-3.

TIP The minimum/maximum rate values can be changed after output ranges have been programmed. The new values are checked against the ranges. If the new values are outside the range boundaries, the new values are not accepted, and the programming error bit is set.

Program Ranges Block

Figure 4.8 shows the format of the Program Ranges programming block. This block programs the following parameters:

- Associated Counter
- Range Type
- Range Number
- Range Start Point
- Range End Point
- Output State

All counters can be running when this block is sent to the module.

Figure 4.8 Program Ranges Block

	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
Word 0	TRMT	0	0	DEBUG	0	RType	CNTR No		0	0	0	1	0	0	0	0
Word 1	Range Number															
Word 2	Range Start Value															
Word 3																
Word 4	Range Stop Value															
Word 5																
Word 6	0	0	0	0	0	0	0	0	Output State							
									Virtual				Real			
Word 7	RESERVED: Must equal zero															

Programming Block Identification Bit (Word 0, Bit 04)

This bit identifies the type of block.

TRMT: Transmit Bit (Word 0, Bit 15)

A 0 to 1 transition starts a programming cycle.

DEBUG: Debug Mode Selection Bit (Word 0, bit 12)

When this bit is set, the debug mode is activated. Debug mode returns the input data file showing current settings in the Program Ranges block. For details, see Debug Mode Operation on page 5-7.

CNTR No.: Counter Number Bits
(Word 0, Bits 08 and 09)

These two bits select the counter to which this programming block is applied. The counter number and range number must correspond to a valid combination as determined by the information in the Module Setup Block. See Range Allocation Values on page 4-8.

Table 4.9 Counter Number Programming Bit Settings

Bit 09	Bit 08	Counter Number
0	0	Counter 1
0	1	Counter 2
1	0	Counter 3
1	1	Counter 4

The valid range of this parameter is dependent on the programmed operating mode.

Rtype: Range Type
(Word 0, Bit 10)

When this bit equals zero, the range specified in this block is a count range. The output state is active when the count value of the associated counter is within the programmed range.

When this bit equals one, the range specified is a rate range. The output state is active when the rate value of the associated counter is within the programmed range.

Range No.: Range Number Bits
(Word 1, Bits 00 to 15)

These bits define which ranges (0-15) will be programmed or reset. If a bit is set (1), the corresponding range is programmed. The number of ranges available is programmed with the range allocation parameters in the Module Setup programming block.

The range number word is subject to the following special conditions:

- If the range start value equals the range stop value and word 6 equals zero, the range indicated is reset.
- If a range or ranges not belonging to the indicated counter are set, the block is rejected and a programming error results.
- If the range number equals zero *and* words two through 7 are equal to zero, all ranges associated with the counter are reset.
- Setting more than one range bit when the values for range start and range stop are different causes a programming error.

TIP Each of the 16 ranges has a unique bit. For example, the ranges allocated for Counter 2 begin sequentially after the ranges for Counter 1.

Range Start Value, Range Stop Value (Words 2 to 5)

When specifying a count range, the range start and range stop values must be within the range of the minimum and maximum count values programmed in the Minimum/Maximum Count Value programming block.

The rate range must be programmed using the same data format as the rate value. If the rate value is specified in floating-point format, the rate range is also. If the rate value is specified in integer format, the rate range is programmed in integer format.

Count values are always in two-word integer format, as described in Integer Format on page 4-3.

If the range start and range stop numbers are *equal*, the range specified by the range number is erased from memory.

Output State: Output State Byte (Word 6, Bits 00 to 07)

This byte defines the state of the outputs while the programmed range is active. It is combined with other output state bytes and output masks to define the actual output states. See Determining Actual

Output State on page 4-27 for a description of how the bytes are combined.

If the start value is less than the stop value, the output state is applied when the count or rate is within the range specified by the two values. (For example, see ranges 1 through 3 on page 2-13.) If the start value is greater than the stop value, the output state is applied when the count or rate is outside the range. (For example, see range 4 on page 2-13.) At least one of these bits must be set when programming a range or a programming error is generated.

Counter Control Block

Figure 4.9 shows the format of the Counter Control programming block. This block allows you to change the state of the following counter controls for all four counters in one cycle:

- Enable/Disable Counter
- Soft Preset (if enabled)
- Internal Direction (if enabled)
- Output ON Mask
- Output Enable Mask
- Count or Rate Value (Class 1 only)
- Enable/Disable Range

All counters can be running when this block is sent to the module.

Figure 4.9 Counter Control Block Format

	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
Word 0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0
Word 1	P1	0	0	0	0	0	0	C/R1	0	0	0	0	0	ID1	SP1	EN1
Word 2	P2	0	0	0	0	0	0	C/R2	0	0	0	0	0	ID2	SP2	EN2
Word 3	P3	0	0	0	0	0	0	C/R3	0	0	0	0	0	ID3	SP3	EN3
Word 4	P4	0	0	0	0	0	0	C/R4	0	0	0	0	0	ID4	SP4	EN4
Word 5	Output Enable Mask								Output ON (OR) Mask							
Word 6	Enable Ranges															
Word 7	RESERVED: Must Equal Zero															

Transmit Bit

The transmit bit is not used. A programming cycle is not needed to program these bits. The block is acted upon for every program scan that bit 07 of word 0 is set. Therefore, a transmit bit is not used.

TIP If an invalid condition exists, the PERR and ACK bits are set and all data in the block is considered invalid.

Programming Block Identification Bit (Word 0, Bit 07)

This bit identifies the type of block.

Control Words (Words 1 to 4)

Each counter has its own control word.

Table 4.10 Control Word Assignments

Control Words	Counter Number
Word 1	Counter 1
Word 2	Counter 2
Word 3	Counter 3
Word 4	Counter 4

In the following programming bits, (n) equals the counter number.

EN*n*: Enable Counter (n) Bit (Words 1 to 4, Bit 00)

On power-up or when the EN(n) bit is reset, the counter is in a frozen state. The counter is free to run when the EN(n) bit is set. All of the counters must be disabled before transmitting a Module Setup programming block. The affected counters must be disabled before transmitting a Counter Configuration programming block. The affected

counter must also be disabled before sending new minimum/maximum count values.

TIP Disabling a counter does not cause an output with the counter to turn off. As long as the count value is within the programming range the output remains active.

TIP Enabling a counter that is not present causes a programming error.

SP*n*: Soft Preset Only (n) Bit
(Words 1 to 4, Bit 01)

When the counter has its gate/preset mode set to any mode except No Preset, the counter is set to its preset value when the corresponding bit makes a 0 to 1 transition. Setting this bit in No Preset mode causes a programming error.

TIP Soft preset does not work when the counter's P(n) bit is changed from 1 to 0 to 1 at the same time that the SP(n) bit is changed from 1 to 0 to 1. For example, when word 1 goes from 8003H to 0000H and back to 8003H, counter 1 is not preset.

ID*n*: Internal Direction (n) Bit
(Words 1 to 4, Bit 02)

When the counter has its input configuration set to Pulse/Internal Direction, the state of this bit determines the direction in which the counter counts. When this bit is reset, the counter increments. When this bit is set, the counter decrements. Setting this bit in other than the Pulse/Internal Direction mode causes a programming error.

C/R(n): Count or Rate Value Bit
(Words 1 to 4, Bit 08)

These bits are only used when the module is configured for Class 1 operation. Depending on the operating mode, the module only transmits the counter's count or rate value. The count value is transmitted when the C/R(n) bit is reset. The rate value is transmitted when the C/R(n) bit is set. When configured for Class 4, setting these bits generates a programming error.

P(n): Program Counter (n) Bit
(Words 1 to 4, Bit 15)

If this bit is reset, bits 1 to 14 must be zero or a programming error results. This bit must be set before the counter control bits are updated for the counter. This allows the user to write 0000H into unused words in the block without inadvertently changing the state of a counter. When this bit is zero, all other bit values in the word are retained inside the module. This affects the soft preset, SP(n), as described in the note on page 4-25.

Output ON (OR) Mask
(Word 5, Bits 00 to 07)

This is a bit pattern which allows the user program to globally turn on outputs, regardless of the programmed ranges and Enable Ranges bytes. When a bit in this byte is zero, the output will turn on based on the programmed ranges, the state of the enable ranges byte, and Output Enable Mask. When this bit is one, the output is on if the corresponding bit in the Output Enable Mask equals one.

Output Enable Mask
(Word 5, Bits 08 to 15)

This is a bit pattern to globally turn off outputs, regardless of the programmed ranges and enable ranges bytes. When a bit in this mask is zero, the output is off regardless of the programmed ranges and the state of the Output ON Mask. When a bit in this mask is one, the

output turns on based on the programmed ranges, the state of the enabled ranges byte, and the Output ON Mask.

TIP The outputs do not turn on if the corresponding bits are not set here.

Enable Range (Word 6)

When a bit in this word is reset (0), the corresponding range (1-16) is disabled, and the output state for the range is ignored.

When a bit in this word is set (1), the corresponding output state for the range is used to determine the state of the eight outputs.

Bits in this word should be zero, unless you want to specifically enable the range.

Determining Actual Output State

The actual state of an output is determined in five steps, as follows:

1. The enable range bits determine if a range should be checked to see if it is active.
2. The output state bytes of all active ranges that are enabled are logically ORed.
3. The Output ON Mask is logically ORed with the results of step 2.
4. The Output Enable Mask is logically ANDed with the results of step 3.
5. The result is applied to the outputs.

IMPORTANT Outputs are always off when the SLC processor is in Program mode. The outputs are only enabled when the processor is in the Run mode.

Outputs not assigned to a counter can only be turned on with the Output ON Mask.

Figure 4.10 Determining Actual Outputs

Range Bit Setting	1	1	0	0	1	1	0	0
Output ON Mask	0	0	0	1	0	0	0	1
Output Enable Mask	0	0	0	0	1	1	1	1
Actual Outputs	0	0	0	0	1	1	0	1

Programming Block Default Values

The following tables list the default values for all of the programmed parameters in each class and operating mode. The default operating mode for each class is mode 1.

Class 1

Table 4.11 Class 1, Mode 1 Default Values

Parameter	Counter 1	Counter 2
Debug Mode Selection	Inactive	
Range Allocation	8	8
Counter Type	Ring	Ring
Input Configuration	X1 Quadrature	X1 Quadrature
Gate/Preset Mode	Store/Preset/Start	Store/Preset/Start
Minimum Count	-32,767	-32,767
Maximum Count	+32,767	+32,767
Minimum Rate	-32,767	-32,767
Maximum Rate	+32,767	+32,767
Preset Value	0	0
All Output Ranges	Not programmed.	
Interrupt Enable	Interrupt disabled	
Rate Value Format	Integer (not programmable)	

Table 4.12 Class 1, Mode 2 Default Values

Parameter	Counter 1	Counter 2	Counter 3
Debug Mode Selection	Inactive		
Range Allocation	8	4	4
Counter Type	Ring	Ring	Ring
Input Configuration	X1 Quadrature	Pulse/Internal	Pulse/Internal
Gate/Preset Mode	Store/Preset/Start	No Preset	No Preset
Minimum Count	-32,767	-32,767	-32,767
Maximum Count	+32,767	+32,767	+32,767
Minimum Rate	-32,767	-32,767	-32,767
Maximum Rate	+32,767	+32,767	+32,767
Preset Value	0	0	0
All Output Ranges	Not programmed.		
Interrupt Enable	Interrupt disabled		
Rate Value Format	Integer (not programmable)		

Table 4.13 Class 1, Mode 3 Default Values

Parameter	Counter 1	Counter 2	Counter 3	Counter 4
Debug Mode Selection	Inactive			
Range Allocation	4	4	4	4
Counter Type	Ring	Ring	Ring	Ring
Input Configuration	Pulse/Internal	Pulse/Internal	Pulse/Internal	Pulse/Internal
Gate/Preset Mode	No Preset	No Preset	No Preset	No Preset
Minimum Count	-32,767	-32,767	-32,767	-32,767
Maximum Count	+32,767	+32,767	+32,767	+32,767
Minimum Rate	-32,767	-32,767	-32,767	-32,767
Maximum Rate	+32,767	+32,767	+32,767	+32,767
Preset Value	0	0	0	0
All Output Ranges	Not programmed.			
Interrupt Enable	Interrupt disabled			
Rate Value Format	Integer (not programmable)			

Class 4

Table 4.14 Class 4, Mode 1 Default Values

Parameter	Counter 1	Counter 2
Debug Mode Selection	Inactive	
Range Allocation	8	8
Counter Type	Ring	Ring
Input Configuration	X1 Quadrature	X1 Quadrature
Gate/Preset Mode	Store/Preset/Start	Store/Preset/Start
Minimum Count	-8,388,607	-8,388,607
Maximum Count	+8,388,607	+8,388,607
Minimum Rate	-1,000,000	-1,000,000
Maximum Rate	+1,000,000	+1,000,000
Preset Value	0	0
All Output Ranges	Not programmed.	
Interrupt Enable	Interrupt disabled.	
Rate Value Format	Integer	

Table 4.15 Class 4, Mode 2 Default Values

Parameter	Counter 1	Counter 2	Counter 3
Debug Mode Selection	Inactive		
Range Allocation	8	4	4
Counter Type	Ring	Ring	Ring
Input Configuration	X1 Quadrature	Pulse/Internal	Pulse/Internal
Gate/Preset Mode	Store/Preset/Start	No Preset	No Preset
Minimum Count	-8,388,607	-8,388,607	-8,388,607
Maximum Count	+8,388,607	+8,388,607	+8,388,607
Minimum Rate	-1,000,000	-1,000,000	-1,000,000
Maximum Rate	+1,000,000	+1,000,000	+1,000,000
Preset Value	0	0	0
All Output Ranges	Not programmed.		
Interrupt Enable	Interrupt disabled.		
Rate Value Format	Integer		

Table 4.16 Class 4, Mode 3 Default Values

Parameter	Counter 1	Counter 2	Counter 3	Counter 4
Debug Mode Selection	Inactive			
Range Allocation	4	4	4	4
Counter Type	Ring	Ring	Ring	Ring
Input Configuration	Pulse/Internal	Pulse/Internal	Pulse/Internal	Pulse/Internal
Gate/Preset Mode	No Preset	No Preset	No Preset	No Preset
Minimum Count	-8,388,607	-8,388,607	-8,388,607	-8,388,607
Maximum Count	+8,388,607	+8,388,607	+8,388,607	+8,388,607
Minimum Rate	-1,000,000	-1,000,000	-1,000,000	-1,000,000
Maximum Rate	+1,000,000	+1,000,000	+1,000,000	+1,000,000
Preset Value	0	0	0	0
All Output Ranges	Not programmed.			
Interrupt Enable	Interrupt disabled.			
Rate Value Format	Integer			

Start Up, Operation, Troubleshooting, and Debug Mode

This chapter provides start up, operation, and troubleshooting information, as well as detailing the operation of the debug mode.

Start Up

The following steps will assist you in the start up of your 1746-HSCE2 module.

1. Install the module in the chassis.
2. Wire the input and output devices.
3. Configure and program your SLC processor to operate with the module.
4. Apply power to the SLC system and to the attached inputs and outputs.

When power is applied to the SLC system, the processor and the module run through a power up diagnostic sequence. After the diagnostics are successfully completed, the SLC processor enters run mode and normal operation begins.

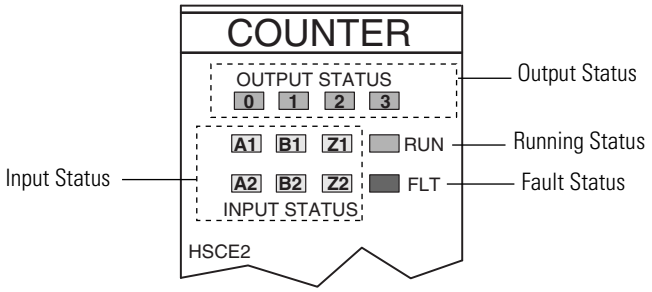
If the SLC processor was in the program mode when power was removed, it returns to the program mode when power is reapplied. Place the SLC processor into run mode using an SLC programming device or keyswitch.

Normal Operation

During normal operation, the LEDs are illuminated as follows:

- The fault LED [FLT] is off.
- LEDs A1, A2, B1, B2, Z1, and Z2 illuminate, indicating the inputs are energized.
- LEDs 1, 2, 3, and 4 illuminate, indicating the status of the physical outputs.
- The run LED is on to indicate the module's running status.

Figure 5.1 LED Locations



Troubleshooting

Three types of module-generated errors can occur:

- module diagnostic errors
- module programming errors
- application errors.

The Fault LED indicates a module diagnostic error.

Fault LED	Problem
Solid Red	Module diagnostic error. Cycle power. If condition persists, replace the module. Refer to "Module Diagnostic Errors" below.
Flashing Red	Module output fuse has been tripped.

The counter status bytes indicate application errors encountered by the module.

Module Diagnostic Errors

A module diagnostic error is produced if the power up self-test or run-time-watchdog test fails. This is an indication of a potential hardware failure.

When it detects a diagnostic error, the module halts all operations. Outputs are reset to zero, and a fault indication is sent to the SLC processor. The module fault LED turns solid red.

In response to a diagnostic error, cycle power. If the condition persists, replace the module.

Module Programming Errors

A programming error is caused by improper set up of a module parameter. The module responds to a programming error by setting the programming error bit. When this bit is set, the entire programming block is rejected.

The programming error bit is set when a reserved bit is set. It is also set under the following conditions:

Table 5.1 Error Conditions by Programming Block

Programming Block	Error Conditions
Module Setup	• Operating mode bits are not set to a valid pattern. • A counter's range allocation value is greater than 16. • The sum of all range allocation values is greater than 16. • The range allocation value for Counter 2 and/or Counter 3 is nonzero and the programmed operating mode has the counter disabled. • A counter or counters were running when the block was sent. • The INT bit was set in Class 1. • The RVF bit was set in Class 1.
Counter Configuration	• Counter number bits are not set to a valid number. (Operating mode may be incorrect.) • Input configuration is invalid for the counter. (Operating mode may be incorrect.) • G/P mode is invalid for the counter. (Operating mode may be incorrect). • The selected counter was running when the block was sent. • The program counter number bits are not set for a counter that has one or more bits set in its corresponding counter setup word.
Min./Max. Count Value	• Counter number bits are not set to a valid number. (Operating Mode may be incorrect.) • The minimum count is outside its valid range. • The maximum count is outside its valid range. • The maximum count is less than or equal to Minimum Count. • Programmed output count ranges are outside the bounds of the new minimum/maximum count values. • The preset value is outside its valid range. • Counter was running when the minimum/maximum count value was changed.

Table 5.1 Error Conditions by Programming Block

Programming Block	Error Conditions
Min./Max. Rate Value	• Counter number bits are not set to a valid number. (Operating Mode may be incorrect.) • The minimum rate is outside its valid range. • The maximum rate is outside its valid range. • The maximum rate is less than or equal to the Minimum Rate. • Programmed output rate ranges are outside the boundaries of the new minimum/maximum rate values. • Rate values may be in the wrong format.
Program Ranges	• The counter number bits are not set to a valid number. (Operating mode may be incorrect.) • The range number is greater than the programmed range allocation value • The range start value is outside its valid range. • The range stop value is outside its valid range. • Range values may be in the wrong format.
Counter Control	• The soft preset bit is set while in No Preset mode. • The internal direction bit is set while not in the internal direction mode. • A counter that is not valid in the selected mode has its enable counter bit set.

Application Errors

The module can encounter the following application errors.

Linear Counter Overflow/Underflow

When the maximum count would be exceeded, the counter overflow bit in the counter status byte is set.

When the count would become one lower than the minimum count, the count underflow bit in the counter status byte is set.

When the module is in overflow condition, the programmed maximum count value is reported and ranges that include the value will still be acted upon. Likewise, in underflow condition, the minimum count value is reported, and ranges including it are affected.

Rate Overflow/Underflow

The rate overflow bit is set when the rate is more than the maximum rate value.

The rate underflow bit is set when the rate value is less than the minimum rate value.

When the module is in overflow condition, the programmed maximum rate value is reported and ranges that include the value will still be acted upon. Likewise, in underflow condition, the minimum rate value is reported, and ranges including it are affected.

Counter Value Does Not Change

Check the LEDs associated with the Channel A and B inputs which have pulses coming in. The A and B LEDs should flash whenever pulses are being received by the 1746-HSCE2 module.

If the A and B LEDs do not flash, check the power to the input sensor and the wiring from the sensor to the module.

If the A and B LEDs flash, make sure that the configuration of the module is complete and counters are enabled.

Counter Value/Rate Value Goes in the Wrong Direction

If single-ended encoder inputs are used, swap channels A and B to change the direction. If differential encoder inputs are used, swap A(+) and A(-) wires.

If pulse and direction inputs are used, check the direction and input type.

If using up and down pulses mode, make sure inputs A and B have not been switched.

Output Does Not Turn On

Make sure the SLC processor is in run mode.

Check the output's LED.

If the LED is illuminated, check the power supply and its connections to the module. Also check the connections to the output device.

If the LED is not illuminated, make sure the SLC processor is in the run mode, and that a module fault has not occurred. Check the output status field of the input image to see if the module is trying to energize the output. If not, make sure that the enable ranges byte and the output OFF mask are set.

Check the fuse status bit.

Output Does Not Turn Off

Check the associated module LED for the output.

If the LED is illuminated, check your program operation.

If the LED is not illuminated, check the wiring to your output device. Check the leakage current of your connected device.

Soft Preset Does Not Work

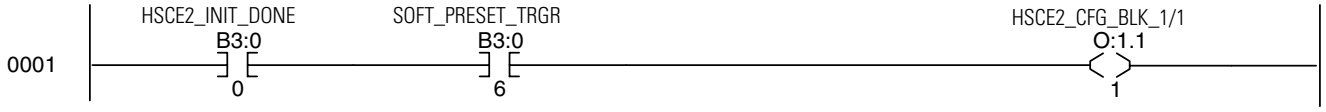
Soft preset does not work when the counter's P(n) bit is changed from 1 to 0 to 1 at the same time that the SP(n) bit is changed from 1 to 0 to 1. For example, when word 1 goes from 8003H to 0000H and back to 8003H, counter 1 is not preset.

Application Programming Errors Affecting Initialization

Typically, ladder logic manipulates 1746-HSCE2 parameters twice. First, the ladder logic initializes the module at power-up using a handshaking procedure shown in Application Examples 1, 2, and 3 in Chapter 6. After initialization, ladder logic can be used to control the 1746-HSCE2 dynamically. For example, the program can manipulate the module's counter preset values (see Example 5 on page 6-18), or the program can soft preset a module counter. The programmer must be very careful to ensure that ladder logic programs intended to manipulate module parameters after initialization do not affect the initialization process.

A typical programming mistake is to use OTE instructions to set 1746-HSCE2 output image bits intended for post-initialization operations (for example, soft presets). OTE instructions set or reset the bit depending on whether the rung conditions are true or false. For example, the following ladder rung sets the bit if the condition is true, meaning bits B3/0 and B3/6 are set. However, it also clears the bit if the rung condition is false, when either B3/0 or B3/6 is reset. The result is that this logic, when scanned, manipulates the module's output image even if it was only intended to run after initialization was complete.

Figure 5.2 OTE Instruction



Most programming errors are easy to locate, since the 1746-HSCE2 error bit (B3/1) is set and the configuration block pointer (N11:0) points at the configuration block during which the error occurred. However, errors that affect initialization are often very difficult to find

due to their unpredictable nature. Even if the configuration block looks satisfactory in the N10 data file, the data block in the module's output image may not be satisfactory.

The best way to check for this problem is to individually search the ladder logic program for all module output words (O:e.0, O:e.1, etc.). Carefully check all ladder logic which manipulates the 1746-HSCE2 output image to ensure that the output image is not corrupted during initialization.

Debug Mode Operation

The debug mode allows you to look at the existing module setup of the programming blocks. When invoked, debug mode echoes back the programming data instead of showing counts and rates in the input data file.

IMPORTANT The Counter Control block does not support the debug mode. Setting the debug bit (word 0, bit 12) in the Counter Control block causes the block to ignore all commands. However, rates and counts continue to be counted. When the debug bit is reset, the module resumes accepting commands.

Activating Debug Mode

Setting the debug bit (word 0, bit 12) in the programming block activates the debug mode. You must also set the block type code, the low byte of word 0, to identify the programming block. The transmit (TRMT), acknowledge (ACK), and programming error (PERR) bit operation is unaffected by debug mode. Depending upon the programming block, other bits may also be required, as described below.

In the Module Setup Block

For the Module Setup Block, the required bits for the debug mode are the transmit bit, the debug bit, and the block type byte. All other bits in the module setup word 0 must be set to 0. Words 1 through 7 are ignored by the module while in debug mode.

Figure 5.3 Required Bits for Module Setup and Counter Configuration Blocks

	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
Word 0	TRMT	0	0	DEBUG	0	0	0	0	BLOCK TYPE							

The debug view of this block shows the range allocation of all four counters. The fourth counter is shown in word 5. The PRA bit (word 0, bit 08) is never set.

In the Counter Configuration Block

The required bits for debug mode in the Counter Configuration Block are the transmit bit, the debug bit, and the block type byte. Bits 13 and 14 must be zero. The values of words 1 through 7 are ignored by the module while in debug mode. The PGM(n) bits (word 0, bits 08 to 11) are never set in this block.

Figure 5.4 Required Bits for Counter Configuration Block

	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
Word 0	TRMT	0	0	DEBUG	0	0	0	0	BLOCK TYPE							

In the Minimum/Maximum Count Value Block

For this block, the transmit bit, the debug bit, the block type byte, and the counter number are required for each configured counter. Word 0 must be used for each configured counter individually. Bit 10 is ignored and bits 11, 13, and 14 must be zero. The values of words 1 through 7 are ignored by the module while in debug mode.

Figure 5.5 Required Bits for Min./Max. Count Value Block

	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
Word 0	TRMT	0	0	DEBUG	0	X	CNTR No.		BLOCK TYPE							

TIP If the counter number entered is not valid, the debug mode returns a programming error.

In the Minimum/Maximum Rate Value Block

For this block, the transmit bit, the debug bit, the block type byte, and the counter number are required for each configured counter. Word 0 must be used for each configured counter individually. Bits 10, 11, 13, and 14 must be zero. The values of words 1 through 7 are ignored by the module while in debug mode.

Figure 5.6 Required Bits for Min./Max. Rate Value Block

	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
Word 0	TRMT	0	0	DEBUG	0	0	CNTR No.		BLOCK TYPE							

TIP If the counter number entered is not valid, the debug mode returns a programming error.

In the Program Ranges Block

To activate the debug mode in the Program Ranges block, the transmit bit, the debug bit, the block type byte, and the range number word (word 1, bits 0 - 15) are required for each range individually. The counter number (word 0, bits 08 and 09) must be zero or a programming error results. The values of any other bits or words 2 through 7 are ignored by the module while in debug mode.

Figure 5.7 Required Bits for Program Ranges Block

	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
Word 0	TRMT	0	0	DEBUG	0	0	0	0	BLOCK TYPE							
Word 1	Range Number															

TIP If more than one bit in word 1 is set (1), the module returns a programming error.

EXAMPLE **Activating Debug Mode**

1. Clear the output image table.
2. Set the required bits in the block that will be echoed back.
3. Set the debug mode bit.
4. Set the transmit bit.

Once the steps above are complete, you can reference the input image words to reflect the block's configuration.

NOTE: Only the first eight words in the input image have meaning in Class 4.

Application Examples

This chapter contains the following application examples:

- Example 1 uses the 1746-HSCE2 in Class 1, mode 3 to count four single-ended, high-speed pulse train inputs using direct addressing only (SLC 5/01™ or SLC 5/02™).
- Example 2 tracks counts and speeds from two quadrature encoders with indirect addressing (SLC 5/03™ and above). The module is used in Class 4, mode 1.
- Example 3 uses the 1746-HSCE2 in Class 1, mode 3 to count two single-ended, high-speed inputs with indexed addressing and the multi-channel high speed counter in a remote I/O chassis (PLC-5® scanner).
- Example 4 illustrates the use of soft presets, expanding on Example 2.
- Example 5 changes presets dynamically using the min/max count block and working from the Example 2 program.
- Example 6 shows how you can use the Min/max Count block preset value to simulate retentive counters, by modifying the Example 2 program.

In these examples, if a programming error occurs (PERR = 1), the error bit (B3:0/1) is set, and N11:0 points to the configuration block that was last sent to the module.

TIP Any parameters which are defaults (see Programming Block Default Values on page 4-28) need not be programmed. For example, if you want all the default values of Class 4 operation, then you only need to configure the module as Class 4 and send a Counter Control block to enable the counters.

The data tables follow the ladder logic. The N10 data table is in hex format to improve readability.

Example 1 - Direct Addressing

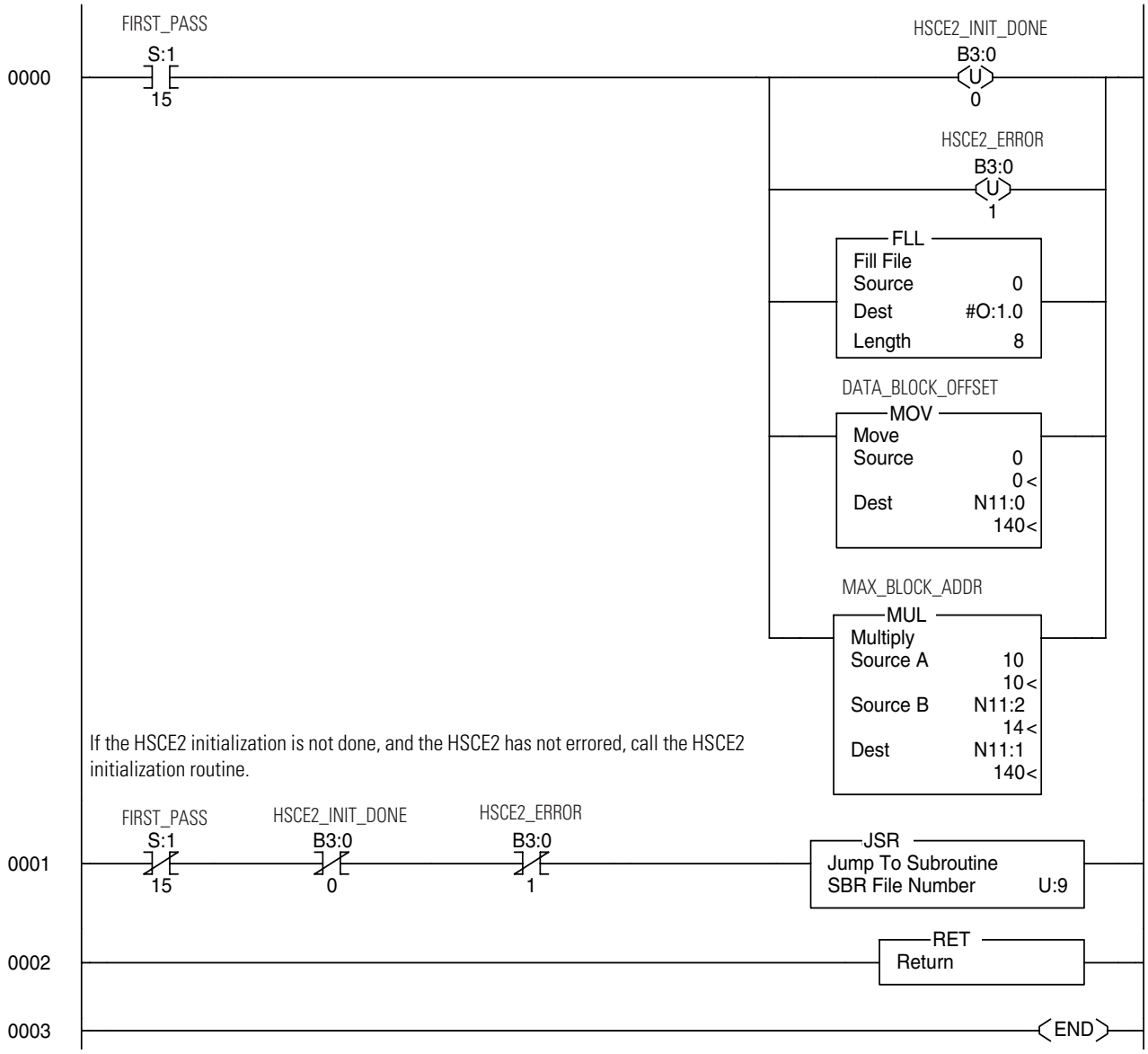
This example sets up the module to count the number of pulses from a high-speed device and apply that information to your ladder program. The module is in Class 1, mode 3, with 4 counters available.

Ladder File 8 - HSCE2

Prior to use, the programmer sets N11:2 to the total number of data blocks which will be entered into file N10 (not including the Counter Control Block), adds one rung for each configuration block (including the Counter Control Block), and initializes the data blocks in file N10. Ten integer data blocks are used (instead of eight) to simplify the display in data windows. Note: The Counter Control Block rung differs from the other rungs because the Counter Control Block does not require hand-shaking.

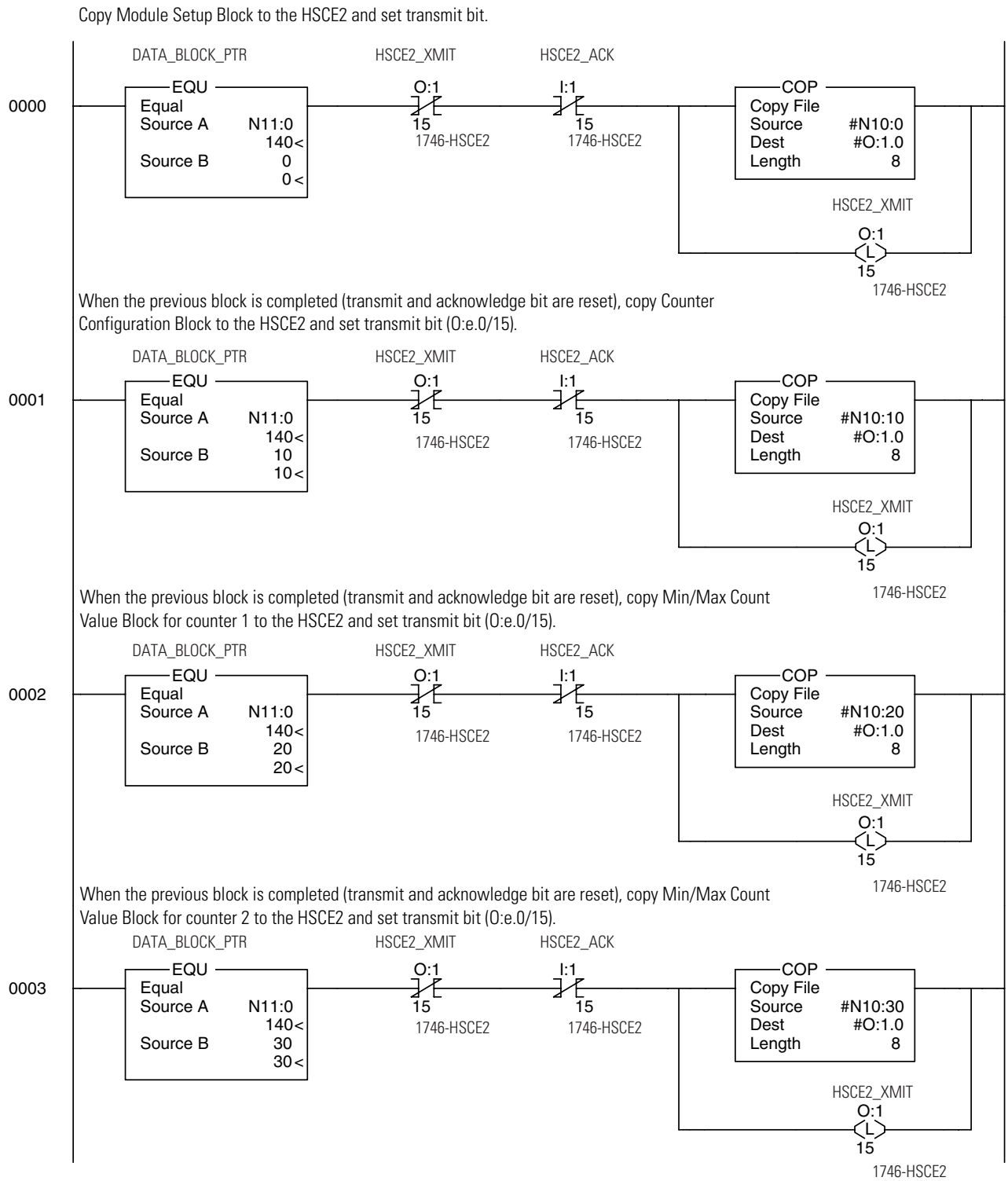
The first pass of the program initializes the following values:

1. The HSCE2 initialization done bit (B3/0) is unlatched.
2. The HSCE2 error bit (B3/1) is cleared.
3. The Counter Configuration Data Block is cleared. Note: The init HSCE2 routine (ladder file 9) is bypassed during the first pass to ensure the Configuration Data Block is reset prior to transfer of the first configuration block
4. The transfer data block offset (N11:0) is cleared; i.e. the first data block starts at offset 0 in N10 file.
5. Max data block address (N11:0) is calculated as: Total Data Blocks (N11:2) x 10 words/data block.

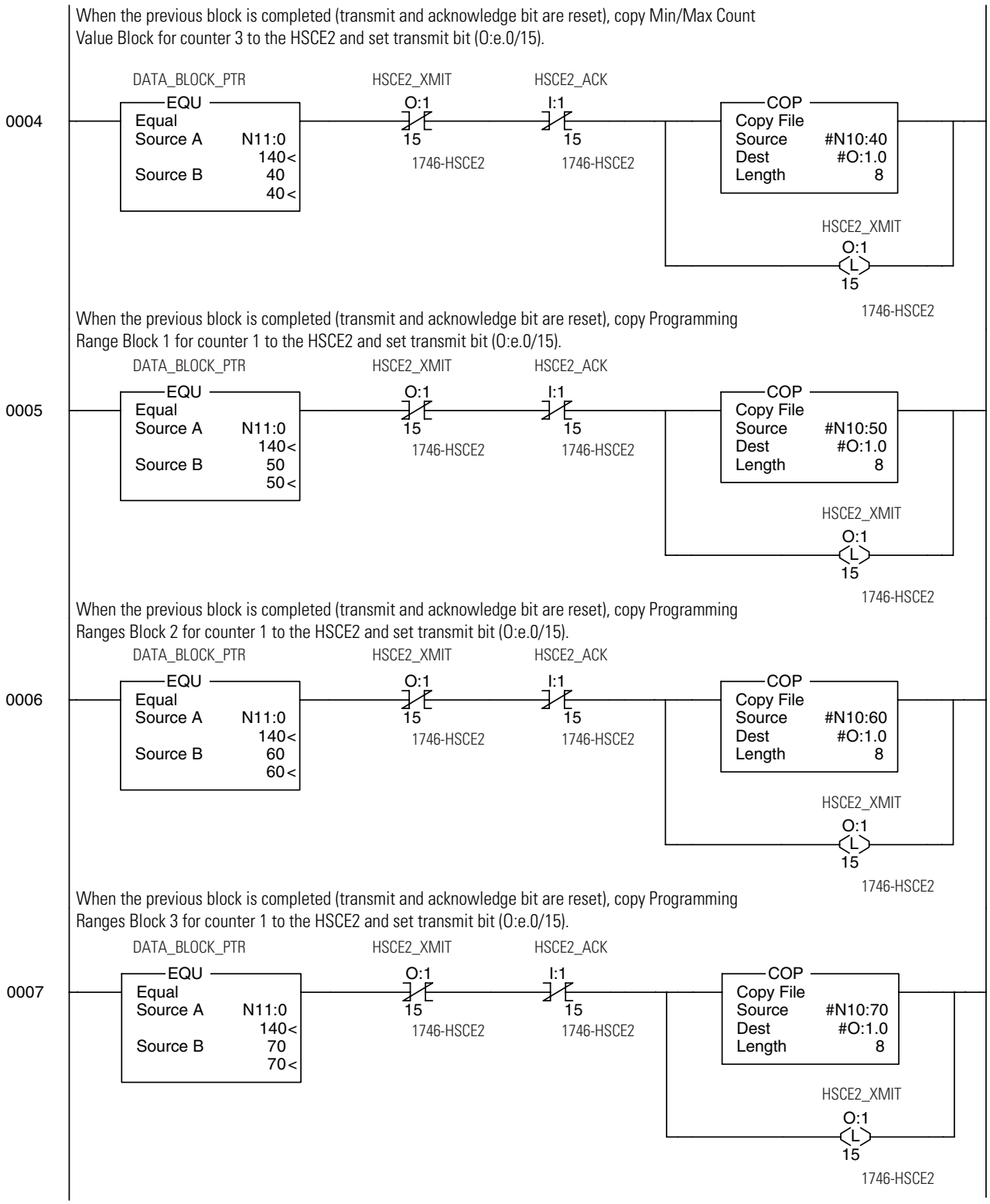


Ladder File 9 - HSCE2 Initialization Routine

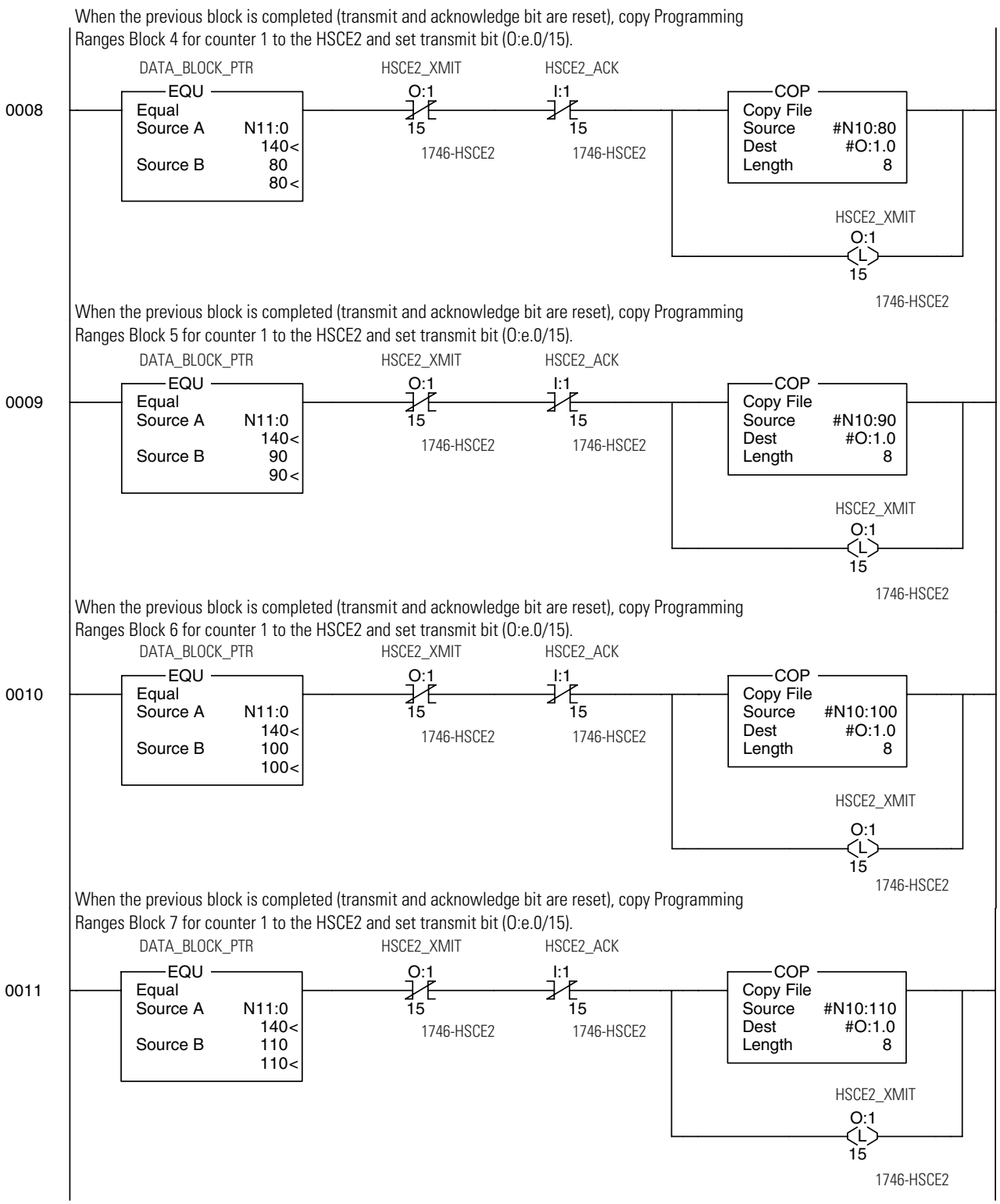
Programming ladder file 9 shows the direct addressing required to set up the programming blocks in this example.



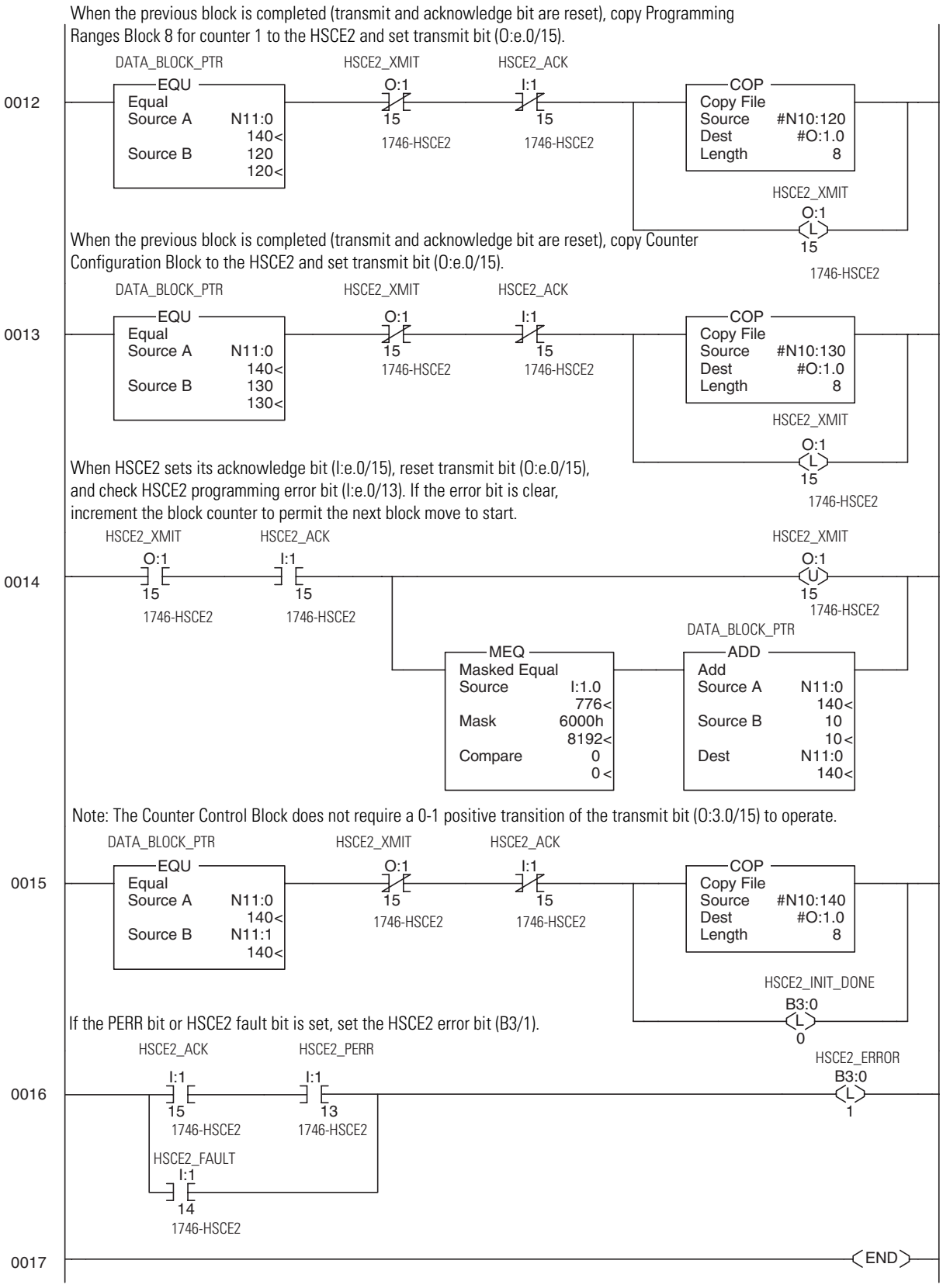
Ladder File 9 Continued



Ladder File 9 Continued



Ladder File 9 Continued



Data Table for N10 File (hexidecimal)

Programming Blocks	Offset	0	1	2	3	4	5	6	7	8	9
Module Setup	N10:0	1	103	8	0	0	0	0	0	0	0
Counter Configuration	N10:10	F02	6	0	6	0	0	0	0	0	0
Min/Max Count Value Counter 1	N10:20	4	0	0	0	190	0	0	0	0	0
Min/Max Count Value Counter 2	N10:30	104	0	0	0	1F4	0	0	0	0	0
Min/Max Count Value Counter 3	N10:40	204	0	0	0	258	0	0	0	0	0
Min/Max Count Value Counter 4	N10:50	304	0	0	0	2BC	0	0	0	0	0
Program Ranges	N10:60	10	1	0	0	0	31	1	0	0	0
Program Ranges	N10:70	10	2	0	32	0	63	2	0	0	0
Program Ranges	N10:80	10	4	0	64	0	95	4	0	0	0
Program Ranges	N10:90	10	8	0	96	0	C7	8	0	0	0
Program Ranges	N10:100	10	10	0	C8	0	F9	1	0	0	0
Program Ranges	N10:110	10	20	0	FA	0	12B	2	0	0	0
Program Ranges	N10:120	10	40	0	12C	0	15D	4	0	0	0
Program Ranges	N10:130	10	80	0	15E	0	190	8	0	0	0
Counter Control	N10:140	80	8001	8001	8001	8001	FF00	FF	0	0	0
	N10:150	0	0	0	0	0	0	0	0		

Data Table for N11 File (decimal)

Offset	0	1	2	3	4	5	6	7	8	9
N11:0	140	140	14							

Example 2 - Indirect Addressing

In this example, the module is set up in Class 4, mode 1 using only two counters. This example uses indirect addressing, which is compatible only with SLC 5/03 or higher processors.

TIP This example may be used with any mode (1, 2, or 3) and with any SLC 5/03 or higher processor, as long as the module is in a local chassis. However, the N10 and N11 data files would need to be modified for a different configuration.

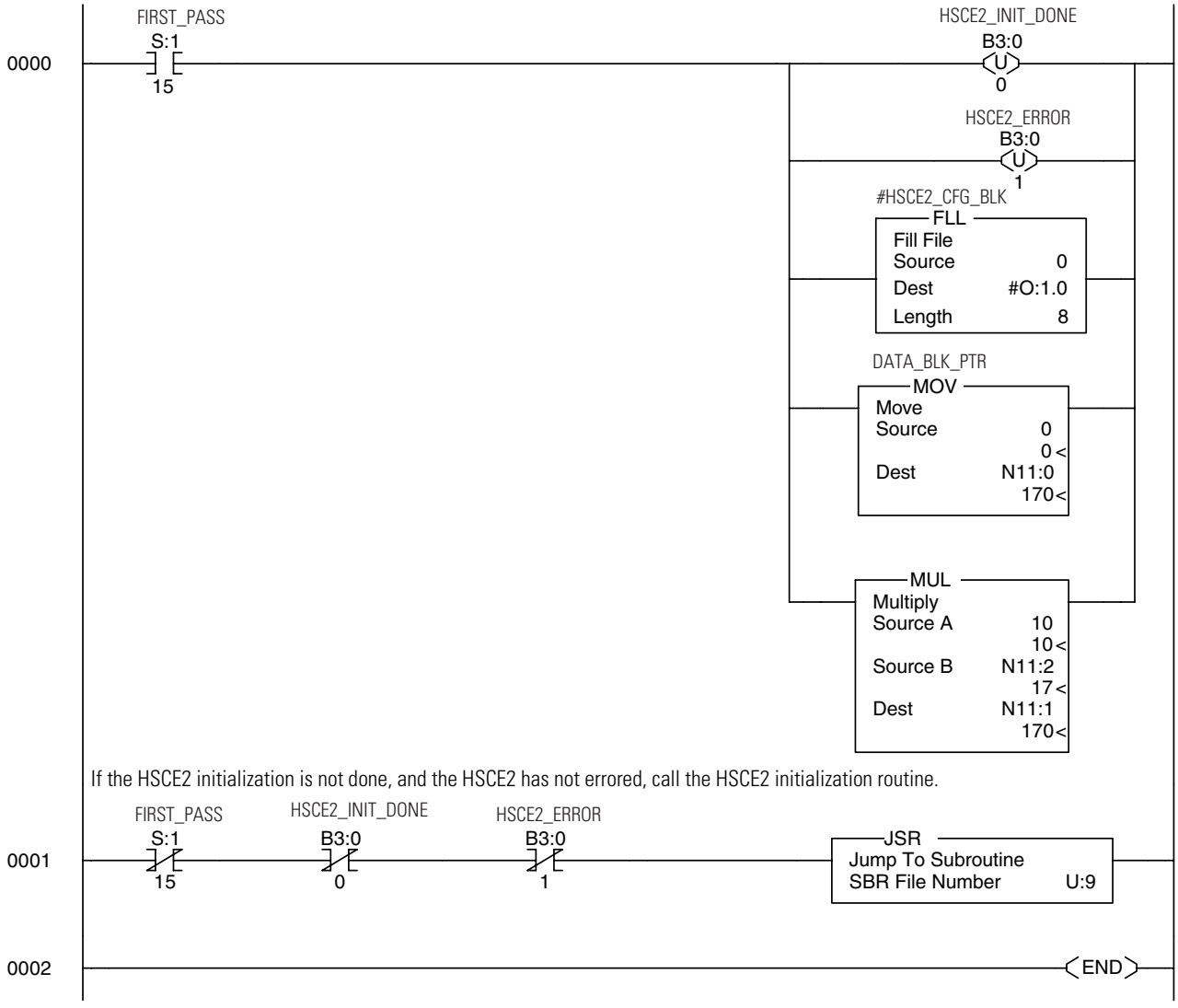
Ladder File 8 - HSCE2

Prior to use, the programmer sets N11:2 to the total number of data blocks which will be entered into file N10 (not including the Counter Control Block), adds one rung for each configuration block (including the Counter Control Block), and initializes the data blocks in file N10. Ten integer data blocks are used (instead of eight) to simplify the display in data windows. Note: The Counter Control Block rung differs from the other rungs because the Counter Control Block does not require hand-shaking.

The first pass of the program initializes the following values:

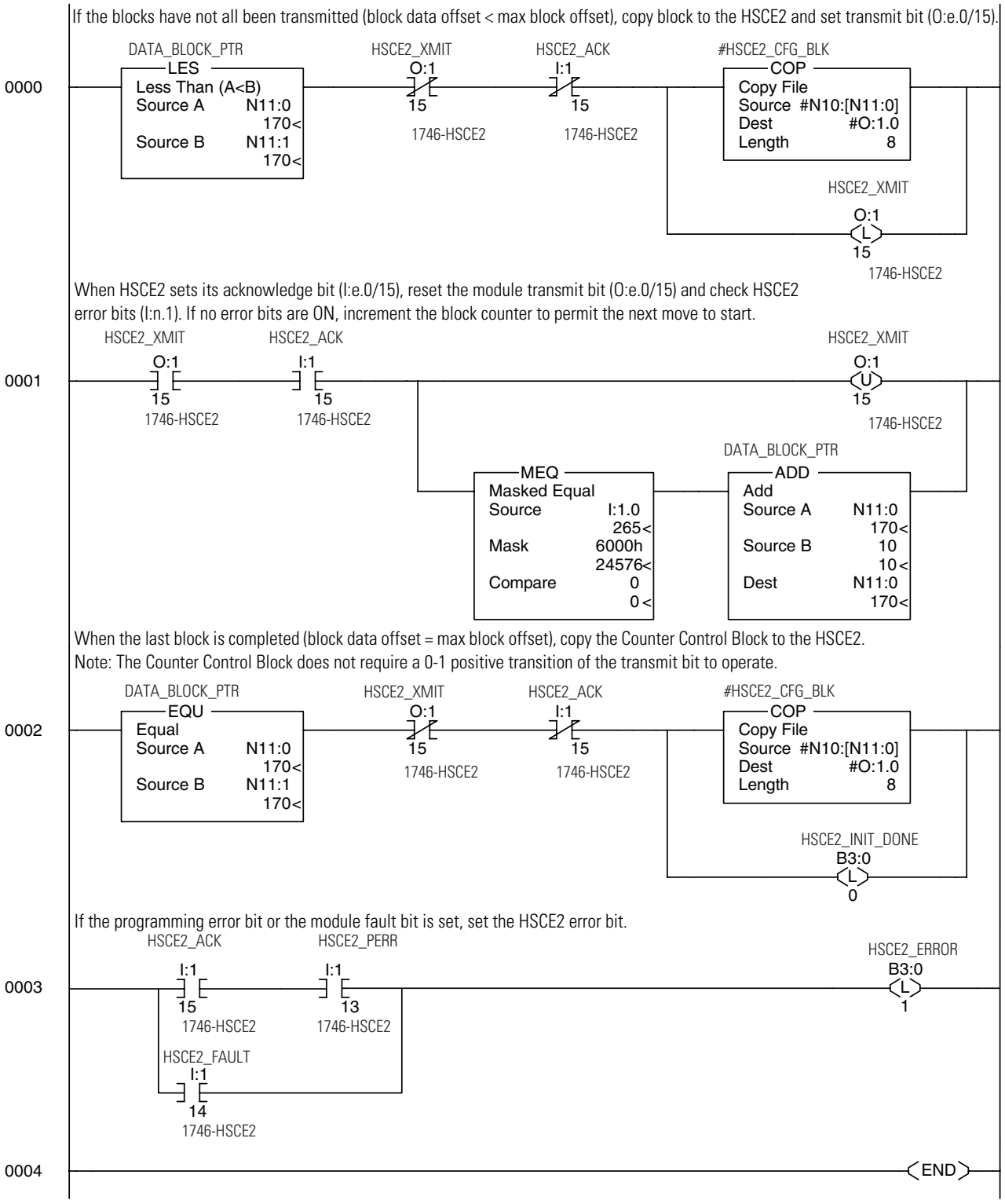
1. The HSCE2 initialization done bit (B3/0) is unlatched.

2. The HSCE2 error bit (B3/1) is cleared.



Ladder File 9 - HSCE2 Initialization Routine

Programming ladder file 9 shows the indirect addressing required to set up the programming blocks in this example.



Data Table for N10 File (hexidecimal)

Programming Blocks	Offset	0	1	2	3	4	5	6	7	8	9
Module Setup	N10:0	1	101	8	0	0	0	0	0	0	0
Counter Configuration	N10:10	302	C	0	C	0	0	0	0	0	0
Min/Max Count Value Counter 1	N10:20	4	0	0	2	30	0	0	0	0	0
Min/Max Count Value Counter 2	N10:30	104	0	0	7	C8	0	0	0	0	0
Min/Max Rate Value	N10:40	8	FF9C	0	64	0	0	0	0	0	0
Program Ranges	N10:50	410	1	0	0	4	3E7	1	0	0	0
Program Ranges	N10:60	410	2	5	0	9	3E7	2	0	0	0
Program Ranges	N10:70	410	4	A	0	E	3E7	1	0	0	0
Program Ranges	N10:80	410	8	F	0	13	3E7	2	0	0	0
Program Ranges	N10:90	410	10	14	0	18	3E7	1	0	0	0
Program Ranges	N10:100	410	20	19	0	1D	3E7	2	0	0	0
Program Ranges	N10:110	410	40	1E	0	22	3E7	1	0	0	0
Program Ranges	N10:120	410	80	23	0	27	3E7	2	0	0	0
Program Ranges	N10:130	110	100	0	0	1	31F	4	0	0	0
Program Ranges	N10:140	110	200	1	320	3	257	8	0	0	0
Program Ranges	N10:150	110	400	3	258	5	18F	4	0	0	0
Program Ranges	N10:160	110	800	5	190	7	C7	8	0	0	0
Counter Control	N10:170	80	8001	8001	0	0	FF00	FFF	0	0	0

Data Table for N11 File (decimal)

Offset	0	1	2	3	4	5	6	7	8	9
N11:0	170	170	17							

Example 3 - Block Transfers

In this example, the module is set up in Class 1, Mode 3 using two counters. This example uses indirect addressing and block transfers with a PLC-5 scanner.

Three rungs are added to ladder file 8, the HSCE2 routine:

1. Repeating block transfer writes (BTW) to send eight words of data to the remote 1746-HSCE2 module.

2. Repeating block transfer reads (BTR) to read eight words of data from the remote 1746-HSCE2 module.

3. A rung to latch the first BTR done bit when it was satisfactory to start the 1746-HSCE2 initialization (ladder file 9).

The 1746-HSCE2 initialization routine (ladder file 9) is nearly the same as the local examples (examples 1 and 2), except the I/O image

addresses (e.g., I:1.0) have been replaced with block transfer data file addresses (e.g., N12:0).

TIP The only changes necessary to permit a different 1746-HSCE2 configuration are to the data files N10 and N11.

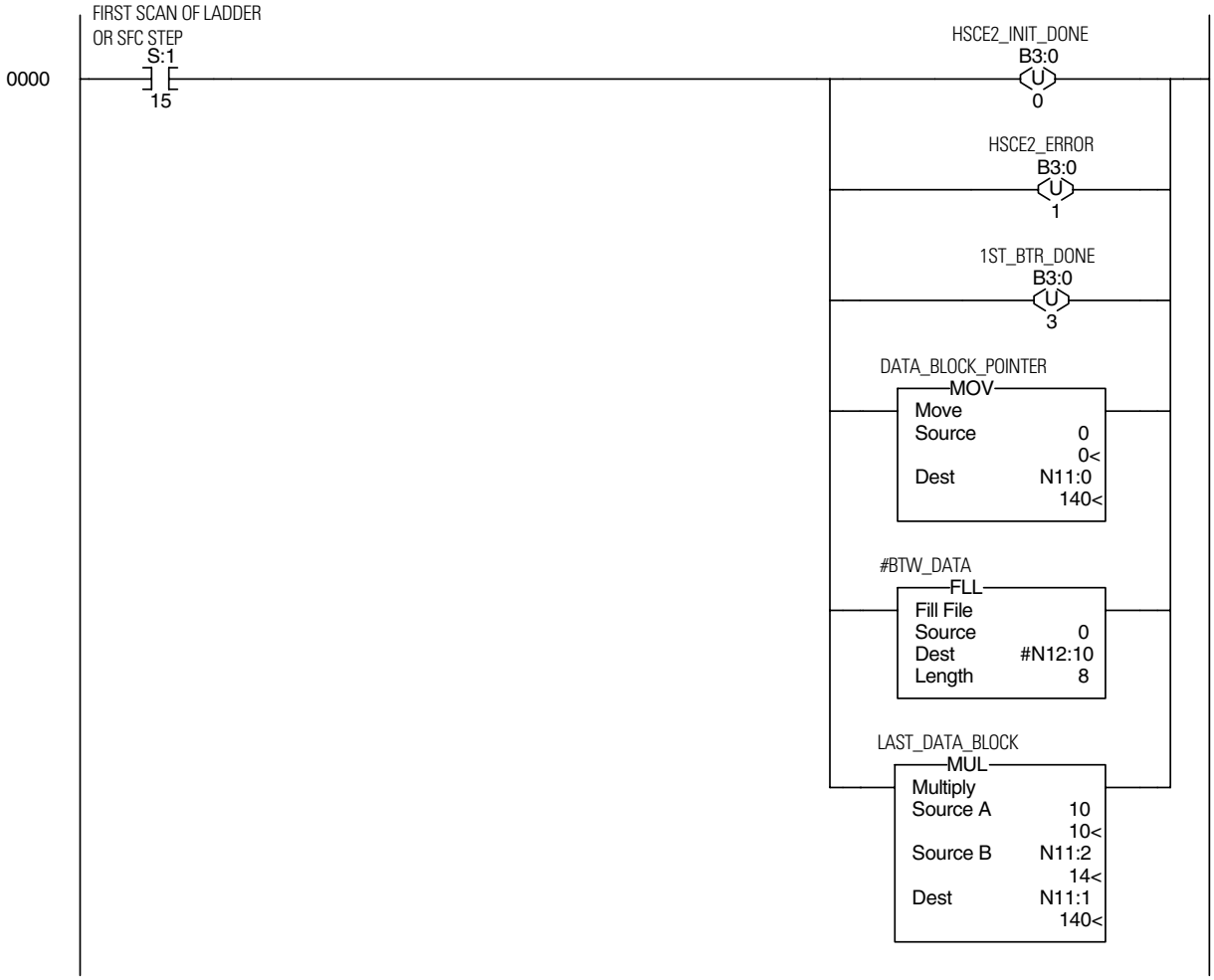
Ladder File 8 - HSCE2

Prior to use, the programmer sets N11:2 to the total number of data blocks which will be entered into file N10 (not including the Counter Control Block), adds one rung for each configuration block (including the Counter Control Block), and initializes the data blocks in file N10. Ten integer data blocks are used (instead of eight) to simplify the display in data windows. The first pass of the program initializes the following values:

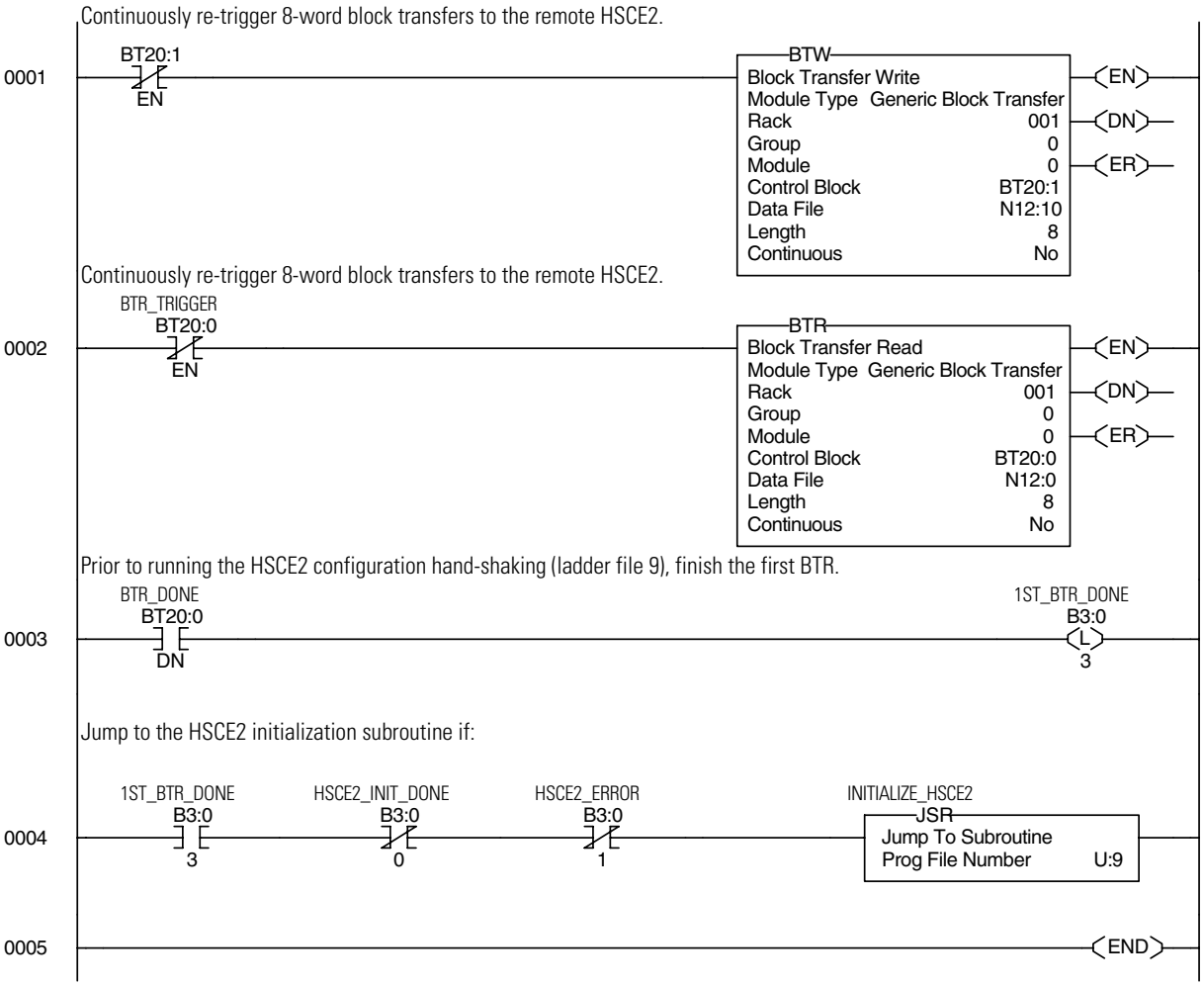
The first pass of the program initializes the following values:

1. The HSCE2 initialization done bit (B3/0) is cleared.

2. The HSCE2 error bit (B3/1) is cleared.

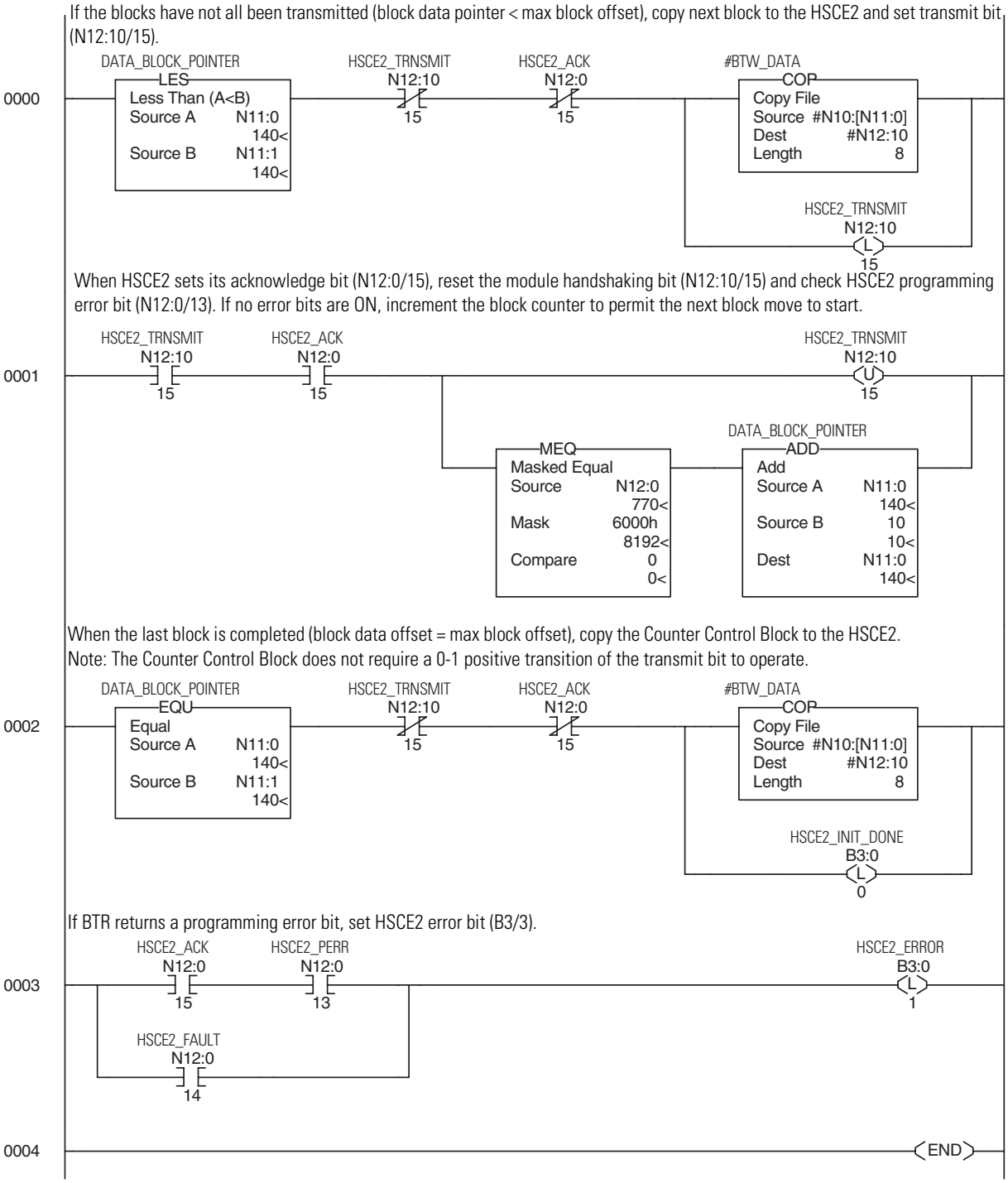


Ladder File 8 Continued



Ladder File 9 - HSCE2 Initialization Routine

Programming ladder file 9 shows the block transfer function required to set up the programming blocks in this example.



Data Table for N10 File (hexidecimal)

Programming Blocks	Offset	0	1	2	3	4	5	6	7	8	9
Module Setup	N10:0	1	103	8	0	0	0	0	0	0	0
Counter Configuration	N10:10	F02	6	0	6	0	0	0	0	0	0
Min/Max Count Value Counter 1	N10:20	4	0	0	0	190	0	0	0	0	0
Min/Max Count Value Counter 2	N10:30	104	0	0	0	1F4	0	0	0	0	0
Min/Max Count Value Counter 3	N10:40	204	0	0	0	258	0	0	0	0	0
Min/Max Count Value Counter 4	N10:50	304	0	0	0	2BC	0	0	0	0	0
Counter 1 Program Ranges	N10:60	10	1	0	0	0	31	1	0	0	0
Counter 1 Program Ranges	N10:70	10	2	0	32	0	63	2	0	0	0
Counter 1 Program Ranges	N10:80	10	4	0	64	0	95	4	0	0	0
Counter 1 Program Ranges	N10:90	10	8	0	96	0	C7	8	0	0	0
Counter 1 Program Ranges	N10:100	10	10	0	C8	0	F9	1	0	0	0
Counter 1 Program Ranges	N10:110	10	20	0	FA	0	12B	2	0	0	0
Counter 1 Program Ranges	N10:120	10	40	0	12C	0	15D	4	0	0	0
Counter 1 Program Ranges	N10:130	10	80	0	15E	0	190	8	0	0	0
Counter Control	N10:140	80	8001	8001	8001	8001	FF00	FF	0	0	0

Data Table for N11 File (decimal)

Offset	0	1	2	3	4	5	6	7	8	9
N11:0	140	140	14	0	256					

Example 4 - Using Soft Presets

This example illustrates the use of soft presets with the Counter Control Block. A soft preset loads the specific counter with a preset count value. This preset value is determined by the last min/max Count Value Block for that counter. This block is normally loaded during HSCE2 initialization, but the preset can be changed dynamically (as shown in Example 5).

1. The ladder logic uses the Example 2 program (SLC 5/03 or higher processor in Class 4, mode 1).

2. The example soft presets Counter 1 whenever the soft preset trigger bit (B3/6) sees a positive (0 to 1) transition.

3. The soft preset must wait until after the HSCE2 initialization process is complete (B3/0 is set).

4. The Counter Configuration Block (N10:10 to N10:17) gate/preset mode for Counter 1 must allow soft presets. In this case, N10:11 was changed from 0C (No Preset) to 1C (Soft Preset Only).

5. The example assumes that the controller control block is in the HSCE2 output image when the soft preset is implemented. Additional logic (for example, preset change latch XIO from example 5) is needed to delay the soft preset logic if other ladder logic changes the output image. (For example, example 5 dynamically changes the preset values and temporarily puts the min/max count value block in the output image.)

6. Rung 3 unlatches the HSCE2 Counter 1 soft preset bit (O:1.1/1) when the soft preset is completed. Since the Counter 1 count value may be changing, we have created a count range using the preset value (N10:25*1000 + N10:26) ± 10 counts to determine if the soft preset is within range. If the Counter 1 count value is static during the soft preset, the ladder logic could simply compare the Counter 1 count value with the preset value.

Ladder File 8 - HSCE2

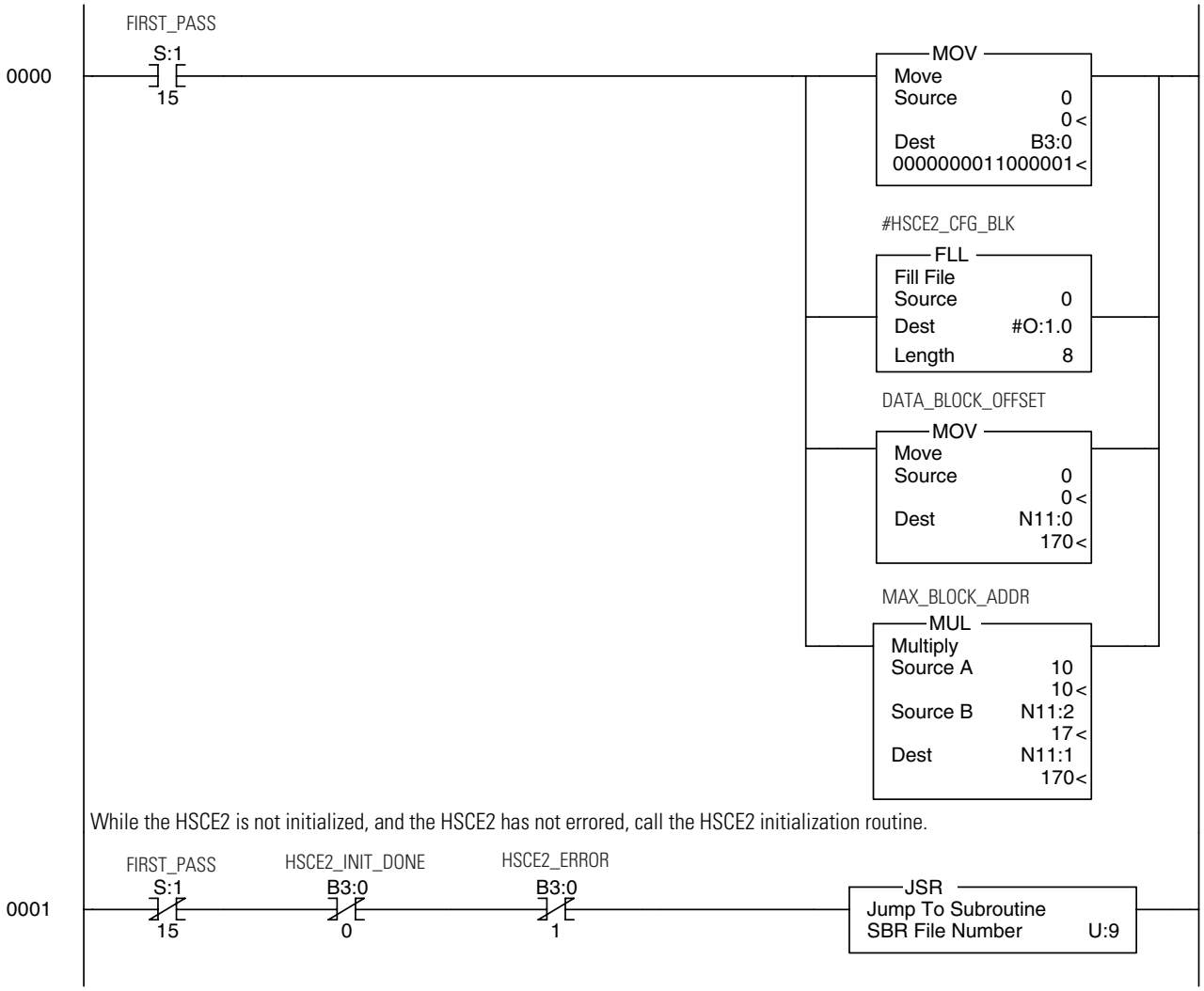
Prior to use, the programmer sets N11:2 to the total number of data blocks which will be entered into file N10 (not including the Counter Control Block) and initializes the data blocks in file N10. Ten integer data blocks are used (instead of eight) to simplify the display in data windows.

The first pass of the program initializes the following values:

1. The HSCE2 initialization done bit (B3/0) is unlatched.

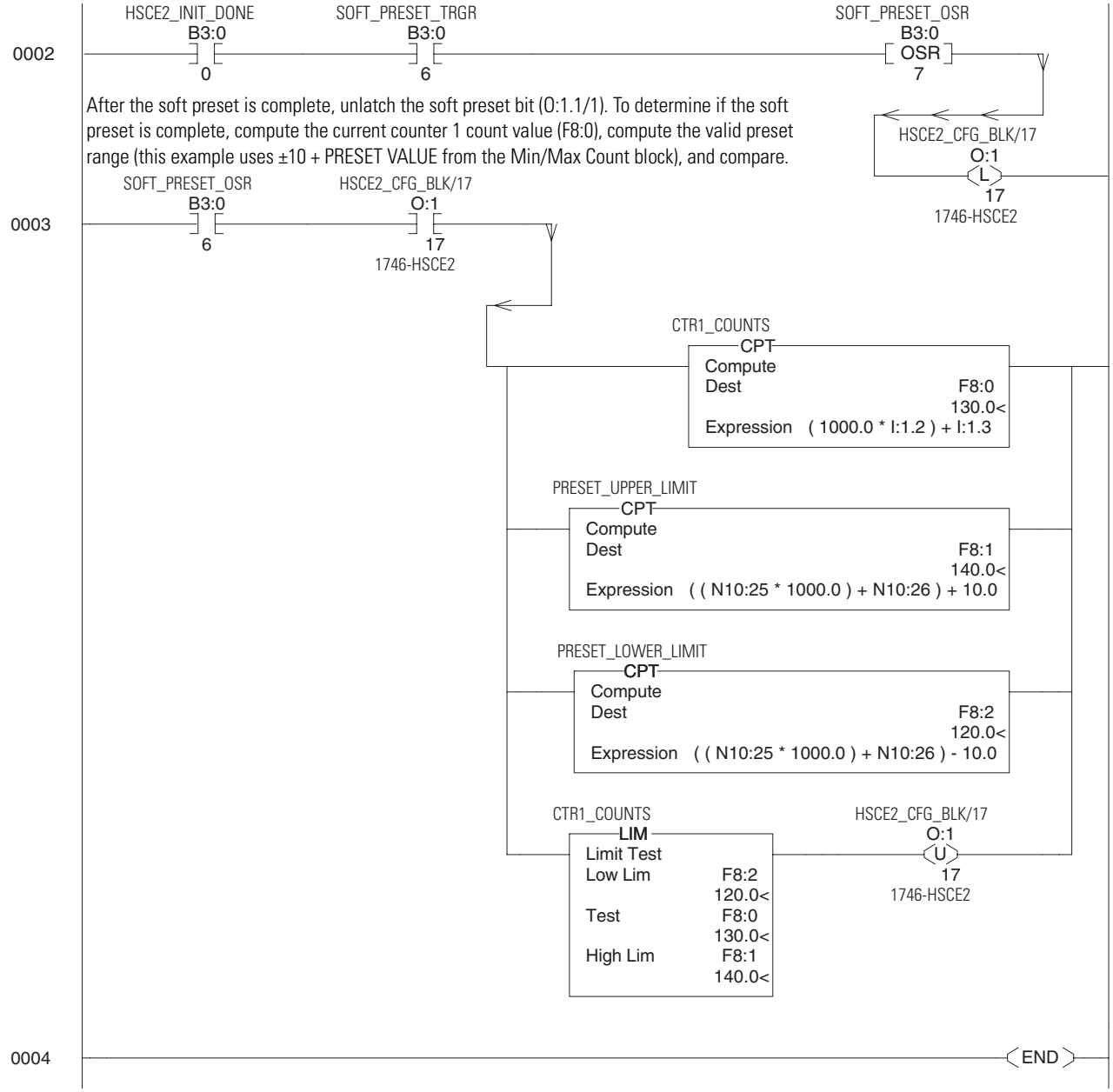
2. The HSCE2 error bit (B3/1) is cleared.

3. The Counter Configuration Block is cleared. Note: The init HSCE2 routine (ladder file 9) is bypassed during the first pass to ensure the Configuration Data Block is reset prior to transfer of the first configuration data block.



Ladder File 8 Continued

This rung implements a soft preset of counter 1 when the soft preset trigger bit sees a positive change (0 to 1). The rung assumes that the Counter Control Block (last configuration block) is still in the output image to the 1746-HSCE2, and that Counter 1 permits soft presets.



Ladder File 9 - HSCE2 Initialization Routine

See the ladder logic from Example 2 on page 6-9.

Data Table for N10 File (hexidecimal)

Programming Blocks	Offset	0	1	2	3	4	5	6	7	8	9
Module Setup	N10:0	1	101	8	0	0	0	0	0	0	0
Counter Configuration	N10:10	302	1C	0	C	0	0	0	0	0	0
Min/Max Count Value Counter 1	N10:20	4	0	0	2	30	0	82	0	0	0
Min/Max Count Value Counter 2	N10:30	104	0	0	7	C8	0	0	0	0	0
Min/Max Rate Value	N10:40	8	FF9C	0	64	0	0	0	0	0	0
Program Ranges	N10:50	410	1	0	0	4	3E7	1	0	0	0
Program Ranges	N10:60	410	2	5	0	9	3E7	2	0	0	0
Program Ranges	N10:70	410	4	A	0	E	3E7	1	0	0	0
Program Ranges	N10:80	410	8	F	0	13	3E7	2	0	0	0
Program Ranges	N10:90	410	10	14	0	18	3E7	1	0	0	0
Program Ranges	N10:100	410	20	19	0	1D	3E7	2	0	0	0
Program Ranges	N10:110	410	40	1E	0	22	3E7	1	0	0	0
Program Ranges	N10:120	410	80	23	0	27	3E7	2	0	0	0
Program Ranges	N10:130	110	100	0	0	1	31F	4	0	0	0
Program Ranges	N10:140	110	200	1	320	3	257	8	0	0	0
Program Ranges	N10:150	110	400	3	258	5	18F	4	0	0	0
Program Ranges	N10:160	110	800	5	190	7	C7	8	0	0	0
Counter Control	N10:170	80	8001	8001	0	0	FF00	FFF	0	0	0

Data Table for N11 File (decimal)

Offset	0	1	2	3	4	5	6	7	8	9
N11:0	170	170	17							

Example 5 - Change Presets Dynamically

This example shows the user how to dynamically change the preset value using the Min/max Count Block.

1. The following procedure uses the Example 2 program (SLC 5/03 or higher processor in Class 4, mode 1).

2. The Min/max Count Value requires the use of handshaking bits to get the preset values into the 1746-HSCE2. Therefore, the handshaking code is in a separate subroutine (ladder file 14). The ladder rungs which trigger the dynamic preset change are in the 1746-HSCE2 routine (ladder file 8).

3. Before and after the Min/max Count Block with the new preset value is transferred to the 1746-HSCE2, the Counter Control Block (with the transmit bit reset), is in the 1746-HSCE2's output image. Leaving the Counter Control Block in the module's output image allows for easy disabling of the counters and implementing of soft presets.

4. Data word N10:11 was changed from 000C (hex) to 001C (hex) to change the Counter 1 gate/preset mode from No Presets (000) to Soft Presets Only (001).

Ladder File 8 - HSCE2

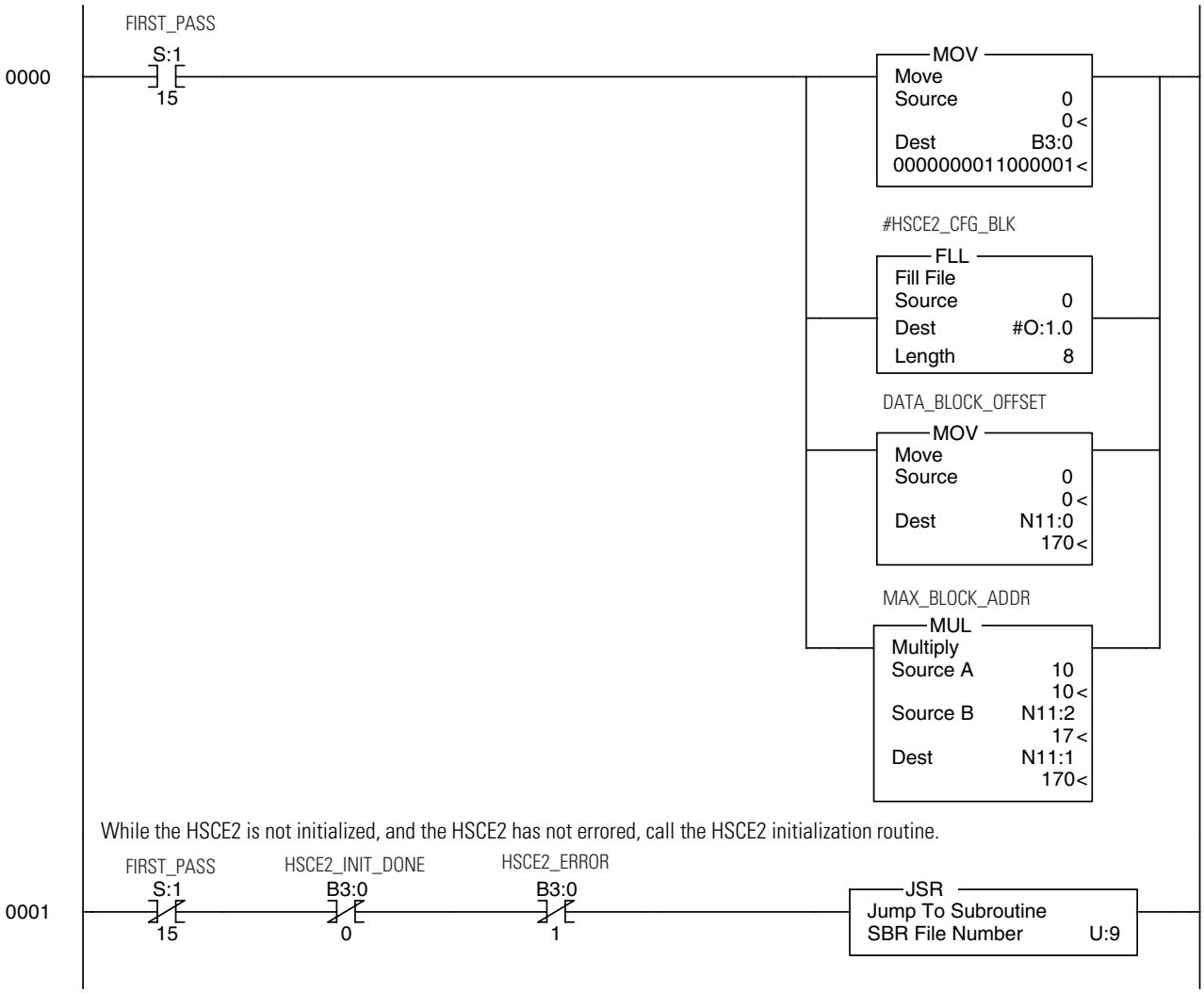
Prior to use, the programmer sets N11:2 to the total number of data blocks which will be entered into file N10 (not including the Counter Control Block) and initializes the data blocks in file N10. Ten integer data blocks are used (instead of eight) to simplify the display in data windows.

The first pass of the program initializes the following values:

1. The HSCE2 initialization done bit (B3/0) is unlatched.

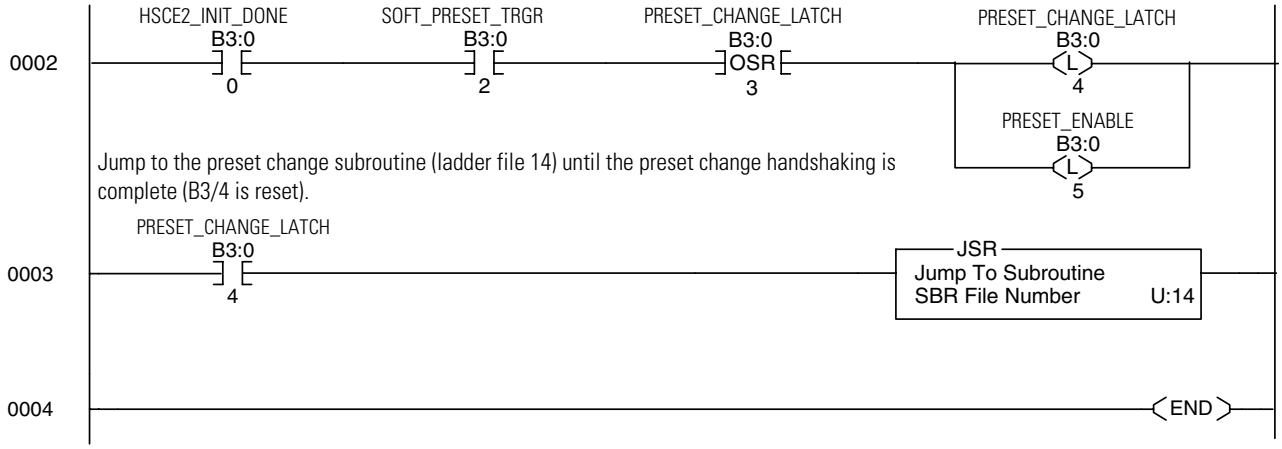
2. The HSCE2 error bit (B3/1) is cleared.

3. The Counter Configuration Block is cleared. Note: The init HSCE2 routine (ladder file 9) is bypassed during the first pass to ensure the Configuration Data Block is reset prior to transfer of the first configuration data block.



Ladder File 8 Continued

This rung triggers a dynamic change of the Counter 1 preset. The preset trigger bit (B3/2) sets the preset change latch bit (B3/4). The preset change latch bit (B3/4) remains latched until the Counter Control Block is restored to the 1746-HSCE2 output image. Use B3/4 to ensure that other logic (soft presets) do not write to the output image until the Counter Control Block is restored. The preset enable bit (B3/5) allows the first handshake rung (ladder file 14, rung 0000) to run just once.

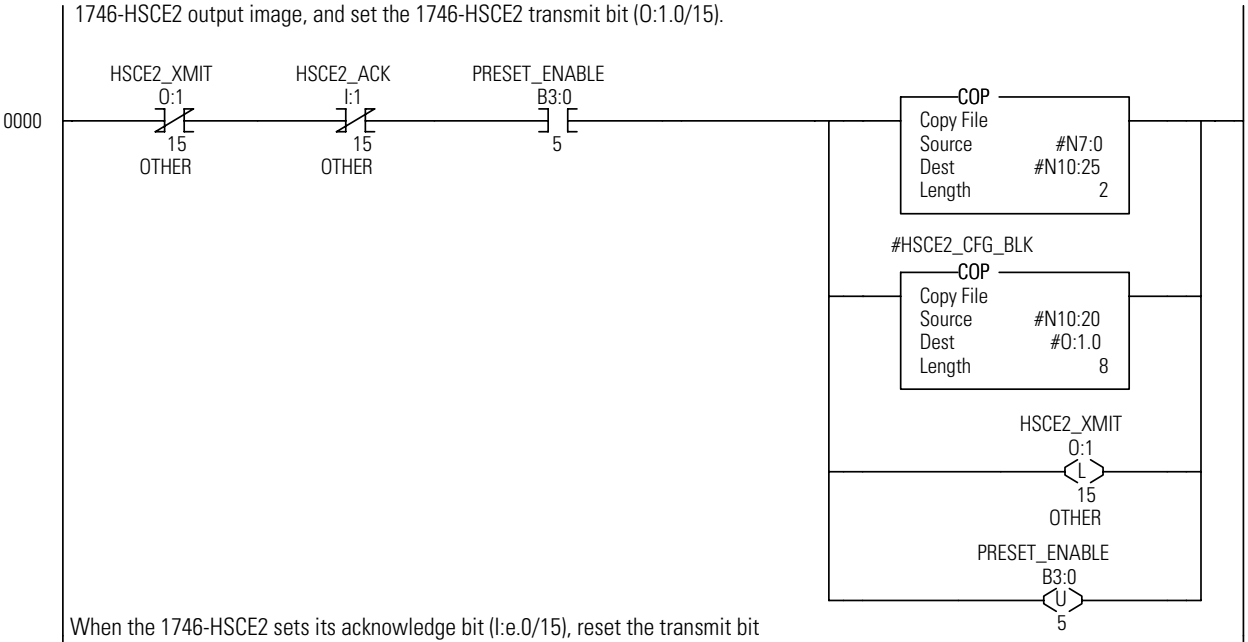


Ladder File 9 - HSCE2 Initialization Routine

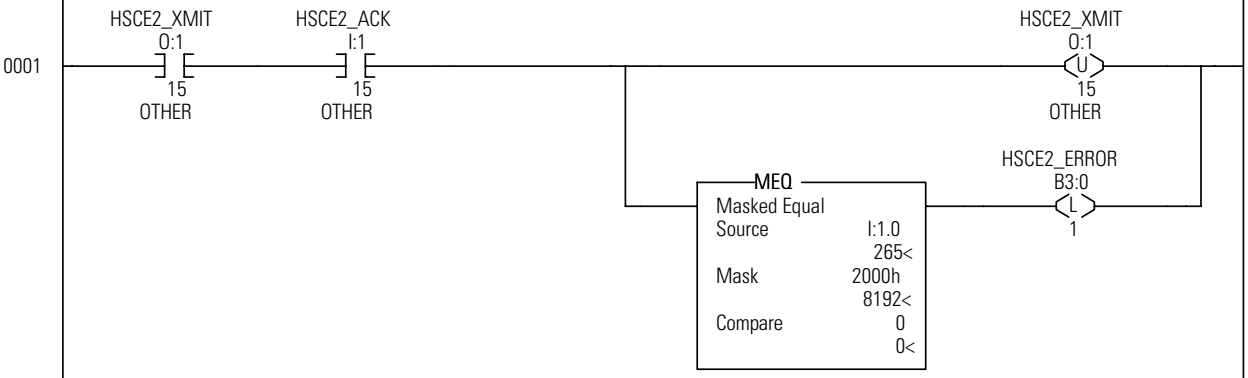
See the ladder logic from Example 2 on page 6-9.

Ladder File 14 - Preset Change Subroutine

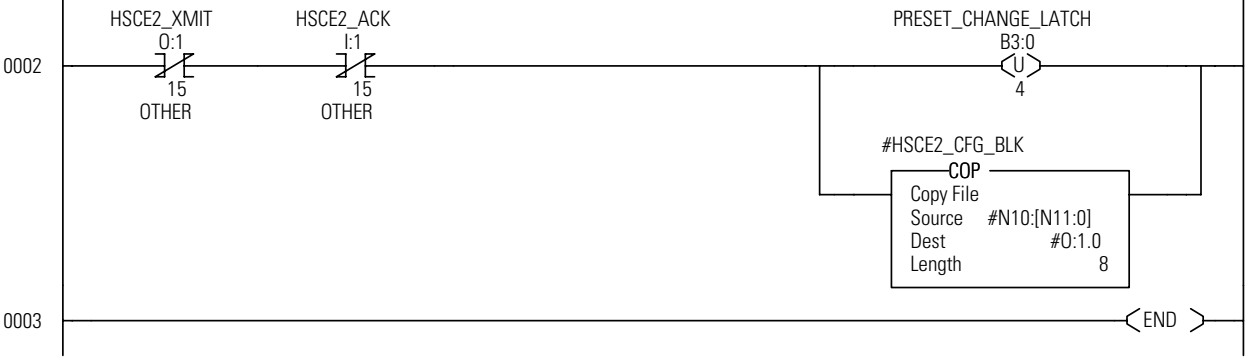
Copy the new preset value (N7:0 and N7:1) into counter 1's min/max count block (N10:25 and N10:26). Copy this block into the 1746-HSCE2 output image, and set the 1746-HSCE2 transmit bit (O:1.0/15).



When the 1746-HSCE2 sets its acknowledge bit (I:e.0/15), reset the transmit bit (O:e.0/15), and check for a programming error.



When the Min/max Count Block transfer is completed, reload the Counter Control Block to the 1746-HSCE2 to permit soft presets, disabling counters, etc.



Data Table for N10 File (hexidecimal)

Programming Blocks	Offset	0	1	2	3	4	5	6	7	8	9
Module Setup	N10:0	1	101	8	0	0	0	0	0	0	0
Counter Configuration	N10:10	302	1C	0	C	0	0	0	0	0	0
Min/Max Count Value Counter 1	N10:20	4	0	0	2	30	0	FA	0	0	0
Min/Max Count Value Counter 2	N10:30	104	0	0	7	C8	0	0	0	0	0
Min/Max Rate Value	N10:40	8	FF9C	0	64	0	0	0	0	0	0
Program Ranges	N10:50	410	1	0	0	4	3E7	1	0	0	0
Program Ranges	N10:60	410	2	5	0	9	3E7	2	0	0	0
Program Ranges	N10:70	410	4	A	0	E	3E7	1	0	0	0
Program Ranges	N10:80	410	8	F	0	13	3E7	2	0	0	0
Program Ranges	N10:90	410	10	14	0	18	3E7	1	0	0	0
Program Ranges	N10:100	410	20	19	0	1D	3E7	2	0	0	0
Program Ranges	N10:110	410	40	1E	0	22	3E7	1	0	0	0
Program Ranges	N10:120	410	80	23	0	27	3E7	2	0	0	0
Program Ranges	N10:130	110	100	0	0	1	31F	4	0	0	0
Program Ranges	N10:140	110	200	1	320	3	257	8	0	0	0
Program Ranges	N10:150	110	400	3	258	5	18F	4	0	0	0
Program Ranges	N10:160	110	800	5	190	7	C7	8	0	0	0
Counter Control	N10:170	80	8001	8001	0	0	FF00	FFF	0	0	0

Data Table for N11 File (decimal)

Offset	0	1	2	3	4	5	6	7	8	9
N11:0	170	170	17							

Example 6 - Retentive Counters

The 1746-HSCE2 configuration and count values are not retentive. If power is cycled to the chassis, the module must be re-initialized and the count value re-entered (preset) if desired. To simulate a retentive counter, the 1746-HSCE2 count values can be read by the processor and "stored" in the Min/max Count Value Block preset value. When the ladder logic re-initialized the module after power-up, the last read count values can be loaded using the Min/max Count Value Block preset value and auto-preset bit. The following example shows how to "store" the count values and use the auto-preset bit to load the preset during 1746-HSCE2 initialization.

1. The following procedure uses the Example 2 program (SLC 5/03 or higher processor in Class 4, mode 1). The ladder logic stores and reloads the Counter 1 count value.

2. The Counter 1 min/max count value block auto-preset bit (N10:20/10) was set to automatically download the preset value during 1746-HSCE2 initialization.

3. Rung 0002 was added to ladder file 8 to copy the Counter 1 count value to the preset value during each program scan.

IMPORTANT The ladder logic will simulate a retentive counter best if the counter is either static or changing slowly during power down. If the Counter 1 count value is changing rapidly, the module's internal count value and the count value in the processor's input image could differ due to the time delays in the system (including 1.5 ms in the module and processor scan time).

Ladder File 8 - HSCE2

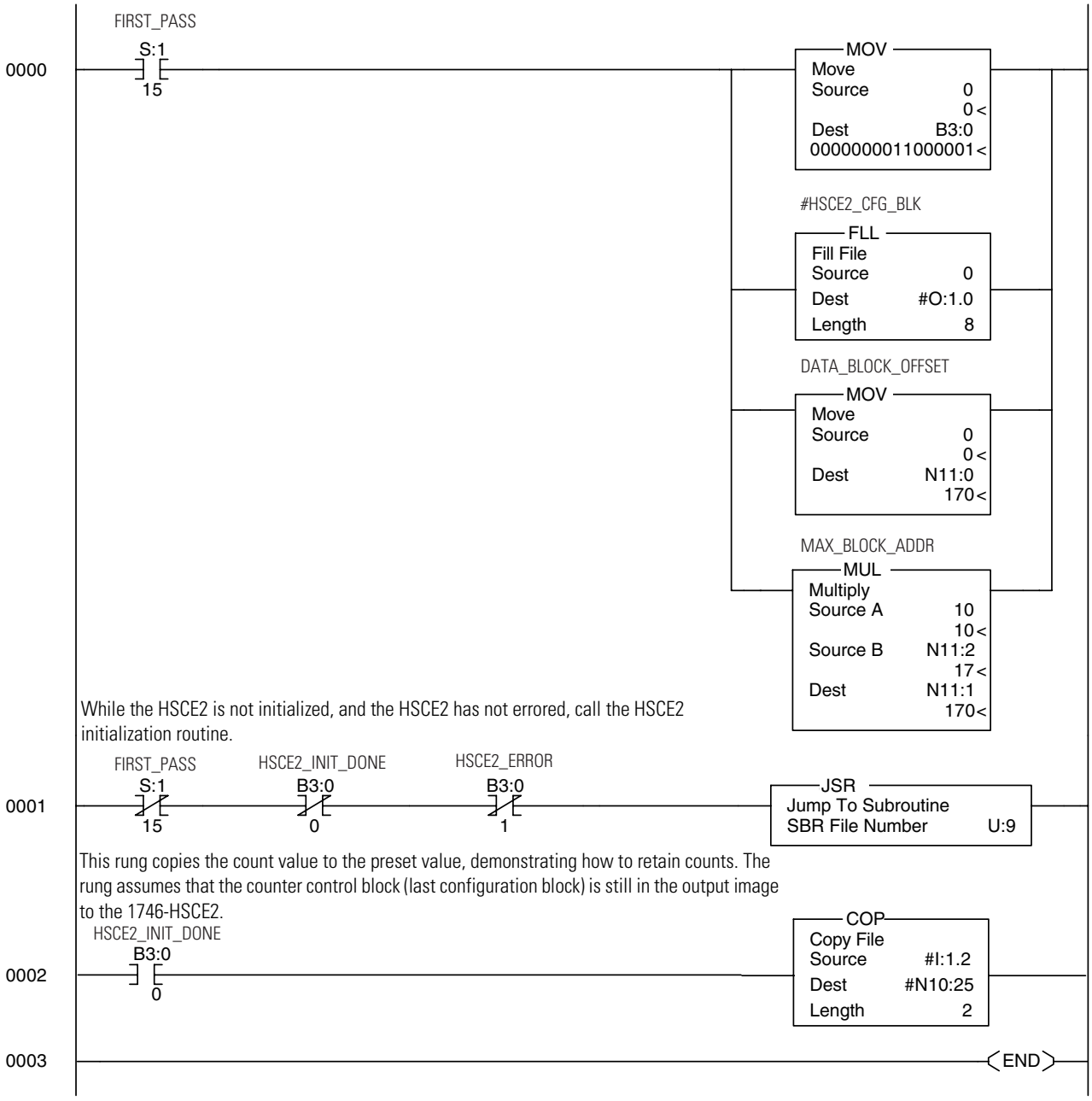
Prior to use, the programmer sets N11:2 to the total number of data blocks which will be entered into file N10 (not including the Counter Control Block) and initializes the data blocks in file N10. Ten integer data blocks are used (instead of eight) to simplify the display in data windows.

The first pass of the program initializes the following values:

1. The HSCE2 initialization done bit (B3/0) is unlatched.

2. The HSCE2 error bit (B3/1) is cleared.

3. The Counter Configuration Block is cleared. Note: The init HSCE2 routine (ladder file 9) is bypassed during the first pass to ensure the



Ladder File 9 - HSCE2 Initialization Routine

See the ladder logic from Example 2 on page 6-9.

Data Table for N10 File (hexidecimal)

Programming Blocks	Offset	0	1	2	3	4	5	6	7	8	9
Module Setup	N10:0	1	101	8	0	0	0	0	0	0	0
Counter Configuration	N10:10	302	1C	0	C	0	0	0	0	0	0
Min/Max Count Value Counter 1	N10:20	4	0	0	2	30	0	82	0	0	0
Min/Max Count Value Counter 2	N10:30	104	0	0	7	C8	0	0	0	0	0
Min/Max Rate Value	N10:40	8	FF9C	0	64	0	0	0	0	0	0
Program Ranges	N10:50	410	1	0	0	4	3E7	1	0	0	0
Program Ranges	N10:60	410	2	5	0	9	3E7	2	0	0	0
Program Ranges	N10:70	410	4	A	0	E	3E7	1	0	0	0
Program Ranges	N10:80	410	8	F	0	13	3E7	2	0	0	0
Program Ranges	N10:90	410	10	14	0	18	3E7	1	0	0	0
Program Ranges	N10:100	410	20	19	0	1D	3E7	2	0	0	0
Program Ranges	N10:110	410	40	1E	0	22	3E7	1	0	0	0
Program Ranges	N10:120	410	80	23	0	27	3E7	2	0	0	0
Program Ranges	N10:130	110	100	0	0	1	31F	4	0	0	0
Program Ranges	N10:140	110	200	1	320	3	257	8	0	0	0
Program Ranges	N10:150	110	400	3	258	5	18F	4	0	0	0
Program Ranges	N10:160	110	800	5	190	7	C7	8	0	0	0
Counter Control	N10:170	80	8001	8001	0	0	FF00	FFF	0	0	0

Data Table for N11 File (decimal)

Offset	0	1	2	3	4	5	6	7	8	9
N11:0	170	170	17							

Specifications

General

Operating Temperature	0°C to +60°C (+32°F to +140°F)
Storage Temperature	-40°C to +85°C (-40°F to 185°F)
Humidity	5 to 95% without condensation
Backplane Current Consumption (power supply loading)	250 mA at +5V dc 0 mA at +24V dc
Backplane Isolation	1000V dc
Maximum Cable Length	300m (1000 ft.)
Agency Certification	UL listed C-UL listed Class 1, Division 2, Groups A, B, C, and D CE certified for all applicable directives C-Tick marked for all applicable acts

Inputs A, B, and Z

Input Voltage	5V dc	24V dc
Input Voltage Range	4.2V dc to 12V dc	10V dc to 30V dc
On-State Voltage (min.)	4.2V	10V
Off-State Voltage (max.)	0.8V	3V
Maximum Off-state Leakage Current	100 µA	100 µA
Input Current (max.)	8 mA	20 mA
Input Current (min.)	6.3 mA	6.3 mA
Nominal Input Impedance	500 Ω	1500 Ω
Min. Pulse Width	475 ns	475 ns
Min. Phase Separation	200 ns	200 ns
Max. Input Frequency	1 MHz	1 MHz
Isolation (from backplane)	1000V	1000V
Isolation (from outputs)	500V	500V

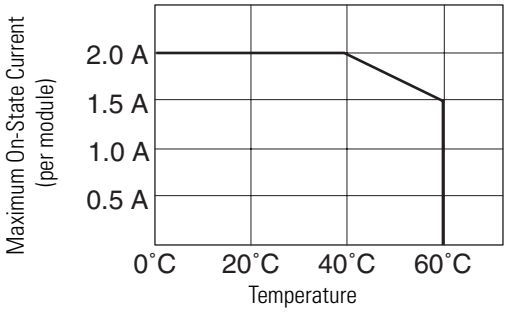
Outputs (sourcing)

Output Voltage Range	5 - 30V dc
Max. On-State Output Current (per channel)	1.0 A at 40°C 1.0 A at 60°C
Max. On-State Current (per module) See the derating graph below.	2.0 A at 40°C 1.5 A at 60°C
Max. On-State Voltage Drop	0.5V
Max. Off-State Leakage Current	100 µA
Isolation (from backplane)	1000V
Isolation (from inputs)	500V

ATTENTION

A transient pulse occurs in transistor output when the external dc supply voltage is applied to the output common terminals (for example, via the master control relay). This can occur regardless of the processor having power or not. For most applications, the energy of this pulse is not sufficient to energize the load. Refer to *SLC 500 Modular Hardware Style User Manual*, publication 1747-UM011, for more information on transient pulses and guidelines to reduce inadvertent processor operation.

On-State Current Derating



Throughput and Timing

Operation	Description	Timing (µs)		
		Minimum	Typical	Maximum
Throughput	The delay between the time the module receives a pulse and when its real outputs and the SLC backplane are updated (based on a count range).	300	700	1600
Input File Update Time	The delay between the time the module receives a pulse and when the backplane count value is updated, including setting the I/O interrupt.	300	600	1500
Output Turn-on Time	The time it takes for the real output to reach 90% output voltage after commanded by the module, not including SLC scan time.	–	–	10
Output Turn-off Time	The time it takes for the real output to reach 10% output voltage after commanded by the module, not including SLC scan time.	–	–	100
Inductive Turn-off Time	The time between the module receiving an input pulse and breaking contact in a BULLETIN 110 contactor.	–	–	50
Rate Accuracy	The accuracy of the reported rate as compared to actual input rate in the equation: reported rate/actual input rate.	–	0.005%	0.015%

Connecting a Differential Encoder

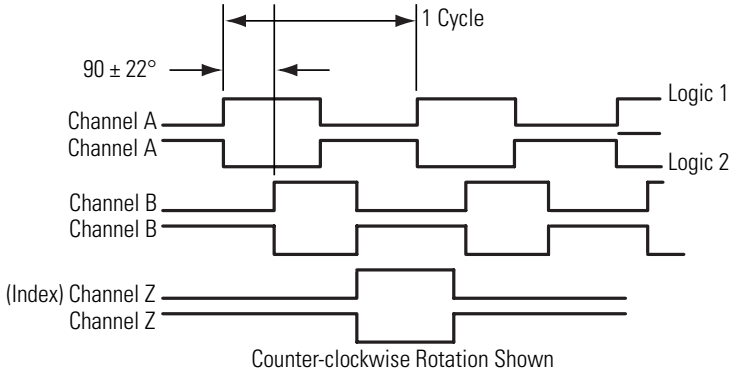
This appendix describes the wiring procedures for connecting a differential encoder to the 1746-HSCE2 module.

For proper module operation, wire the encoder so that the Z input signal is high (true) at the same time the A and B input signals are low (false). If this condition is not met, inconsistent homing may occur.

If you are using an Allen-Bradley Bulletin 845H differential encoder, this condition is met by following the wiring diagrams in the manual. The following five steps describe how to connect a differential encoder to the module.

1. Obtain the encoder output timing diagram from the encoder data sheets. The timing diagram for the 845H encoder is shown below for example purposes only.

Figure B.1 845H Encoder Timing Diagram



2. Look at the Z input signal and its complement Z signal on the timing diagram. Whichever signal is low for most of the encoder revolution and pulses high for the marker interval should be wired into the Z(+) terminal. The remaining signal should be wired into the Z(-) terminal.

3. Look at the B input signal and its complement B signal. Whichever signal is low for at least part of the marker interval should be wired to the B(+) terminal. If both signals meet this condition, either signal may be wired to the B(+) terminal. Wire the remaining signal to the B(-) terminal.

4. Look at the A input signal and its complement A signal. Whichever signal is low for at least part of the marker interval should be wired to the A(+) terminal. If both signals meet this condition, then either signal may be wired to the A(+) terminal. Wire the remaining signal to the A(-) terminal.

5. Since the encoder may be mounted on either end of a motor shaft, the encoder may spin clockwise or counter-clockwise for a given shaft direction. As a result, the direction (phasing) of the encoder may be backwards. If this is the case, exchange the A(+) wire with the A(-) wire.

Module Programming Quick Reference

The module programming blocks are duplicated below for your reference. A column has been added to show corresponding hex values.

Figure C.1 Module Setup Block (see pages 4-6 to 4-10)

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00		Hex Format			
TRMT	0	0	DEBUG	0	0	0	0	0	0	0	0	0	0	0	1	**Word 0**	(1)	0	0	1
0	0	0	0	0	INT	RVF	PRA	0	0	0	0	0	0	Op Mode		**Word 1**	0		0	
0	0	0	0	0	0	0	0	0	0	0	Counter 1 Range Allocation					**Word 2**	0	0		
0	0	0	0	0	0	0	0	0	0	0	Counter 2 Range Allocation					**Word 3**	0	0		
0	0	0	0	0	0	0	0	0	0	0	Counter 3 Range Allocation					**Word 4**	0	0		
RESERVED: Must equal 0																**Word 5**	0	0	0	0
RESERVED: Must equal 0																**Word 6**	0	0	0	0
RESERVED: Must equal 0																**Word 7**	0	0	0	0

(1) 0 for normal operation. 1 for debug mode.

Figure C.2 Counter Configuration Block (see pages 4-10 to 4-13)

	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00		Hex Format			
All Counters	TRMT	0	0	DEBUG	PGM4	PGM3	PGM2	PGM1	0	0	0	0	0	0	1	0	**Word 0**	(1)		0	2
Counter 1	0	0	0	0	0	0	0	0	0	G/P Mode			Input Config			CType	**Word 1**	0	0		
	0																**Word 2**				
Counter 2	0	0	0	0	0	0	0	0	0	G/P Mode			Input Config			CType	**Word 3**	0	0		
	0																**Word 4**				
Counter 3 or 4 as indicated	0	0	0	0	0	0	G/Pmode	CType	0	0	0	0	0	0	G/Pmode	CType	**Word 5**	0		0	
	Counter 4								Counter 3												
	0																**Word 6**				
	0																**Word 7**				

(1) 0 for normal operation. 1 for debug mode.

Figure C.3 Minimum/Maximum Count Value Block (see pages 4-13 to 4-16)

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00		Hex Format			
TRMT	0	0	DEBUG	0	AUTO PRESET	CNTR No		0	0	0	0	0	1	0	0	**Word 0**	(1)		0	4
Upper 4 digits: Minimum Count Value																**Word 1**				
Lower 3 digits: Minimum Count Value																**Word 2**				
Upper 4 digits: Maximum Count Value																**Word 3**				
Lower 3 digits: Maximum Count Value																**Word 4**				
Upper 4 digits: Preset Value																**Word 5**				
Lower 3 digits: Preset Value																**Word 6**				
RESERVED: Must equal zero																**Word 7**	0	0	0	0

(1) 0 for normal operation. 1 for debug mode.

Figure C.4 Minimum/Maximum Rate Value Block (see pages 4-16 to 4-19)

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00		Hex Format			
TRMT	0	0	DEBUG	0	0	CNTR No		0	0	0	0	1	0	0	0	**Word 0**	(1)		0	8
Minimum Rate Value in integer or floating point notation																**Word 1**				
																Word 2				
Maximum Rate Value in integer or floating point notation																**Word 3**				
																Word 4				
RESERVED: Must equal zero																**Word 5**	0	0	0	0
RESERVED: Must equal zero																**Word 6**	0	0	0	0
RESERVED: Must equal zero																**Word 7**	0	0	0	0

(1) 0 for normal operation. 1 for debug mode.

Figure C.5 Program Ranges Block (see pages 4-19 to 4-23)

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00		Hex Format			
TRMT	0	0	DEBUG	0	RType	CNTR No		0	0	0	1	0	0	0	0	**Word 0**	(1)		1	0
Range Number																**Word 1**				
Range Start Value																**Word 2**				
																Word 3				
Range Stop Value																**Word 4**				
																Word 5				
0	0	0	0	0	0	0	0	Output State								**Word 6**	0	0	0	0
								Virtual				Real								
RESERVED: Must equal zero																**Word 7**	0	0	0	0

(1) 0 for normal operation. 1 for debug mode.

Figure C.6 Counter Control Block (see pages 4-23 to 4-28)

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00		Hex Format			
0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	**Word 0**	0	0	8	0
P1	0	0	0	0	0	0	C/R1	0	0	0	0	0	ID1	SP1	EN1	**Word 1**			0	
P2	0	0	0	0	0	0	C/R2	0	0	0	0	0	ID2	SP2	EN2	**Word 2**			0	
P3	0	0	0	0	0	0	C/R3	0	0	0	0	0	ID3	SP3	EN3	**Word 3**			0	
P4	0	0	0	0	0	0	C/R4	0	0	0	0	0	ID4	SP4	EN4	**Word 4**			0	
Output Enable Mask								Output ON (OR) Mask								**Word 5**				
Enable Ranges																**Word 6**				
RESERVED: Must equal zero																**Word 7**	0	0	0	0

Frequently Asked Questions

This appendix presents some of the more commonly asked questions about application and operation of the Multi-channel High Speed Counter Module. The following questions and answers do not cover all possible questions, but are representative of the more common ones.

Q: What happens when my processor faults?

A: All outputs will turn off. In a remote chassis, the status of the outputs when the processor faults is dependent upon the last state bit.

Q: What happens to my outputs if I place the processor in program mode?

A: All outputs turn off. The inputs remains active and the module keeps counting. When the processor is returned to RUN mode, all defaults are restored.

Q: What does it mean when the indicator for a particular input is on.

A: If the indicator is on, it means that input voltage is present. If the indicator is off, the input is floating or has no voltage.

Q: What does it mean when an output indicator is on?

A: Since the output indicator is tied to the logic side of the module, it means that the module has commanded the output on. It does not necessarily mean that the output is on. The indicator illuminates even when no connection is made to the outputs or to the output supply. For an output to actually turn on, the output power supply must be connected.

Q: What are the delay times for turning the outputs on and off?

A: The outputs turn on in < 10 µs, and turn off in < 100 µs. However, overall throughput is between 300 µs and 1.5 ms. Throughput is the delay time between the module receiving a pulse and the updating of its real outputs and the SLC backplane.

Q: Can I connect all of my outputs to the same output device?

A: Any or all of the 4 module outputs can go to the same output device, as long as the output commons and Vcc are the same and the total output current is less than 1.5 A.

Q: Can I connect all of my inputs to the same input device?

A: You can if the device supplies enough current to drive multiple inputs.

Q: How does the module make rate calculations?

A: See Rate Value on page 2-10.

Q: How do I know what length to make my block transfer read/write (BTR/BTW) file?

A: The BTR/BTW blocks should always consist of 8 input/output words.

Comparing 1746-HSCE2 to 1746-HSCE

	1746-HSCE High Speed Counter	1746-HSCE2 Multi-Channel High Speed Counter
Number of Counters	1	2 to 4
Counter Capability	16-bit (±32,767)	24-bit (±8,388,607)
Operating Class	Class 3 only.	Class 1 or Class 4.
Input Voltage	2.8 to 5.5V dc	4.2 to 30V dc
Output Current	0.125 A	1.0 A
Input Frequency Response	50K Hz	1M Hz
Backplane Response Time	60 ms	0.7 to 1.6 ms
Module Compatibility	Uses M-files. Not compatible with SLC5/01 and 5/02 or 1747-ASB.	Supports handshaking. Compatible with SLC 5/01 and 5/02 and 1747-ASB.(1)
Rate Periods	Programmable.	Self-determined.
Sequence Mode	24-step	n/a
Count/Rate Modes	12 ranges	16 ranges
Preset Inputs	Multiple preset inputs for 1 counter. Hard preset disable.	1 preset input for counters 1 and 2 only. No preset input for counters 3 and 4. No hard preset disable.

(1) In Class 1 only.

The following terms and abbreviations are used throughout this manual. For definitions of terms not listed here refer to *Allen-Bradley's Industrial Automation Glossary*, Publication AG-7.1.

class

The class of the module (Class 1 or Class 4) determines: (1) its compatibility with various processors; (2) the number of I/O words; (3) its interrupt ability; and (4) the limits for the count and rate values.

debug mode

A mode of operation that allows the user to view the current configuration settings in the input data file instead of showing counts or rates.

dynamic parameter

A configuration parameter that can be altered while the counter is running.

gate/preset mode

The gate/preset mode determines what, if any gating is applied to the counter and what conditions, if any, preset the counter to the preset value.

input configuration

Input configuration determine how the A and B inputs cause the counter to increment or decrement.

operating mode

The operating mode determines the number of available counters and which inputs are attached to them.

overflow (counter)

The module's status when the maximum count would be exceeded.

overflow (rate)

The module's status when the maximum rate is exceeded.

rate period

The interval, in time or in counts, during which pulses are counted.

rate value

The counts per second (Hz) value that the module reports to the processor.

real outputs

The actual physical outputs on the module.

static parameter

A parameter that must not be altered while the counter is running.

underflow (counter)

The module's status when the count value would be less than the minimum value.

underflow (rate)

The module's status when the rate value is less than the minimum value.

virtual output

The status bits within the module that are set by module's program and can be examined by the user program.

A

C

D

N

O

P

R

S

T

U

V

W

X

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For an additional level of technical phone support for installation, configuration and troubleshooting, we offer TechConnect Support programs. For more information, contact your local distributor or Rockwell Automation representative, or visit http://support.rockwellautomation.com.

Installation Assistance

If you experience a problem with a hardware module within the first 24 hours of installation, please review the information that's contained in this manual. You can also contact a special Customer Support number for initial help in getting your module up and running:

United States	1.440.646.3223 Monday – Friday, 8am – 5pm EST
Outside United States	Please contact your local Rockwell Automation representative for any technical support issues.

New Product Satisfaction Return

Rockwell Automation tests all of its products to ensure that they are fully operational when shipped from the manufacturing facility. However, if your product is not functioning and needs to be returned:

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